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Military Products Data Catalog

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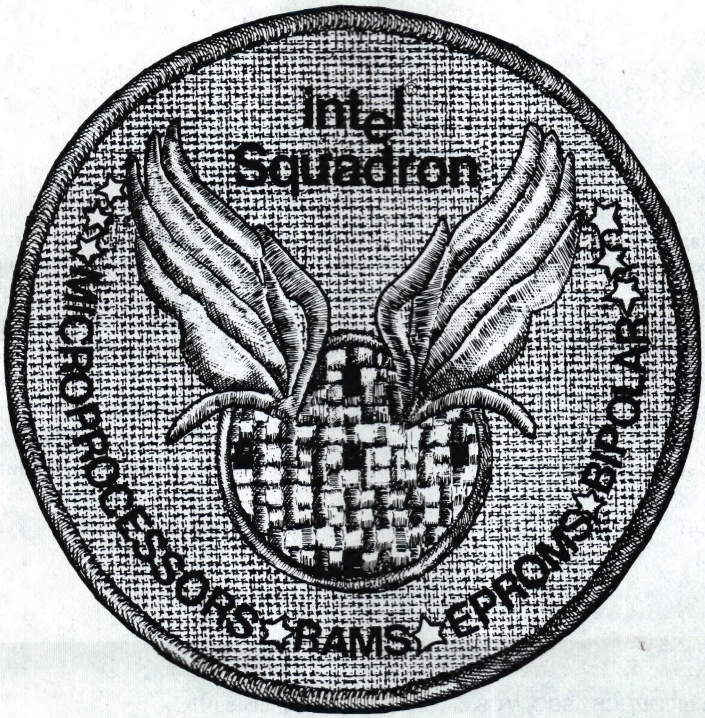


January 1981

Additional copies of this manual or other Intel literature may be obtained from:

Literature Department
Intel Corporation
3065 Bowers Avenue
Santa Clara, CA 95051

FOREWORD

A rapidly increasing number of military and hi-rel applications are turning toward microprocessor based architectures and high density memory components, taking advantage of the benefits of size, economy, performance and reliability. This demand for high technology LSI products with proven reliability is a natural extension of Intel's historic capabilities.

Intel offers a broad line of LSI components processed and tested to military standards. All standard products are screened to full Class B requirements of MIL-STD-883B, Method 5004. Additionally, complete quality conformance testing is performed in accordance with MIL-STD-883B, Method 5005.

Intel will continue to demonstrate its commitment to the military/hi-rel market by upgrading the latest breakthroughs in high performance LSI/VLSI technology to military standards. Also, as slash sheets are issued, Intel plans to support additional JAN qualifications.

In 1977, Intel qualified the first military microprocessor under MIL-M-38510. The JAN version of the industry standard 8080A is listed in Part I of the Qualified Products List (QPL-38510) as M38510/42001BQB.

Every effort is made to adopt the processing and performance standards set by official military specifications. Table I lists the available versions of each product:

MIL-M-38510: Products qualified to MIL-M-38510 and listed in QPL-38510.

Example:	**Part number**	**Marking**
	M38510/42001BQB	JM38510/42001BQB

883/CLASS B: Intel's standard military product with full Class B processing per MIL-STD-883B, Methods 5004 and 5005.

Example:	**Part number**	**Marking**
	MD2716	MD2716/B

DESC SPEC: Class B products screened to DESC Selected Item Drawing (issued by Defense Electronics Supply Center). DESC specs become obsolete when QPL source for JAN product becomes available.

Example:	**Part number**	**Marking**
	7802201JB	7802201JB MD2716/B

MIL TEMP ONLY (MTO): Standard commercial processing, guaranteed to meet Intel military data sheet electrical specifications across the rated temperature range. Must be special ordered.

Example:	**Part number**	**Marking**
	MD2716 S8311	MD2716 S8311

TABLE I

MILITARY PRODUCTS

Product	Mil Temp Only (S-spec No.)	883/ Class B	Desc Selected Item Drawing	JAN (MIL-M-38510/XXX)
M2114A-4	S8399	X		
M2114A-5	S8400	X		
M2114AL-3	S8401	X		
M2114AL-4	S8402	X		
M2118-4	S8403	X		
M2118-7	S8379	X		
M2147H	S8404	X		238*
M2147H-3	S8405	X		238*
M2148H	S8406	X		
M2716	S8311	X	78022	
M2732	S8376	X	80012*	
M3636	S8375	X		210*
M8048		X		490*
M8748		X		
M8035L		X		
M8080A	S8027	X		420
M8212	S8035	X		
M8214	S8036	X		
M8216	S8037	X		
M8224	S8028	X		
M8226	S8038	X		
M8228	S8029	X		
M8085A	S8370	X	79010	
M8155	S8374	X		
M8755A		X		
M8086	S8368	X		530*
M8282	S8375	X		
M8283		X		
M8284	S8372	X		
M8286	S8373	X		
M8287		X		
M8288	S8371	X		
M8251A		X		
M8253		X		
M8255A	S8032	X		
M8257		X		
M8259A		X		

*Pending—Call nearest Intel sales office for information.

General Requirements	MIL-M-38510 Requirements	JAN (Class B)	883 (Class B)
CERTIFICATION			
A. Product Assurance Program Plan	Para. 3.4.1.2	X	MIL-STD-883 Requirements Apply
B. Manufacturer's Certification	Para. 3.4.1.2.1	X	
DEVICE QUALIFICATION	Para. 4.4	X	
TRACEABILITY	Para. 3.4.6	X	
COUNTRY OF MANUFACTURE	Para. 3.2.1	X	
Screening Test Requirements	**Screening Per Method 5004 of MIL-STD-883**		
INTERNAL VISUAL	2010, Cond. B	100%	100%
STABILIZATION BAKE	1008, Cond. C (24 Hrs. @ 150°C)	100%	100%
TEMPERATURE CYCLING	1010, Cond. C (10 cycles −65°C to +150°C)	100%	100%
CONSTANT ACCELERATION	2001, Cond. D or E As Applicable	100%	100%
SEAL (HERMETICITY)			
A. Fine	1014, Cond. B (5×10^{-8} atm-cc/sec)	100%	100%
B. Gross	Cond. C		
PRE BURN-IN ELECTRICAL	Per Applicable Device Specification	100%	100%
BURN-IN	1015, Cond. C or D (160 Hrs. @ 125°C)	100%	100%
FINAL ELECTRICAL TESTS			
A. Static (@ 25°C, Min and Max Rated Temp)	Per Applicable Device Specification	100%	100%
B. Functional and Switching (@25°C, Min and Max Rated Temp)	Per Applicable Device Specification	100%	100%
EXTERNAL VISUAL	2009	100%	100%
Quality Conformance Inspection Tests	**Per MIL-STD-883, Method 5005**	**JAN (Level B)**	**883 (Level B)**
GROUP A Electrical Tests	Per Applicable Device Specification. Table I, Subgroups as Required	Every Inspection Lot	Every Inspection Lot
GROUP B Package Function and Mechanical Tests	Per Table IIb, Subgroups 1-3	Every 6 Weeks	Every 6 Weeks
GROUP C Die Related Tests	Per Table III, Subgroups 1 and 2	Every 12 Weeks	Every 12 Weeks
GROUP D Package Related Tests	Per Table IV, Subgroups 1-5	Every 6 Months	Every 6 Months

Table of Contents

CHAPTER 1

Memory Products

CHAPTER 2

Microcomputer Components

Memory Products

1

M2114A
1024 X 4 BIT STATIC RAM

MILITARY

	M2114AL-3	M2114AL-4	M2114A-4	M2114A-5
Max. Access Time (ns)	150	200	200	250
Max. Current (mA)	50	50	70	70

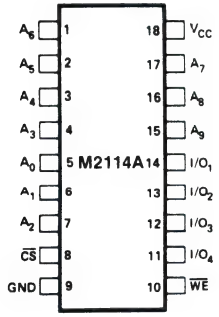
- **HMOS Technology**
- **Low Power, High Speed**
- **Identical Cycle and Access Times**
- **Single +5V Supply ±10%**
- **High Density 18 Pin Package**
- **Completely Static Memory - No Clock or Timing Strobe Required**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **M2114 Upgrade**
- **Military Temperature Range -55° C to +125° C**

The Intel® M2114A is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using HMOS, a high performance MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, therefore it requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

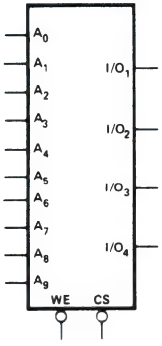
The M2114A is designed for memory applications where the high performance and high reliability of HMOS, low cost, large bit storage, and simple interfacing are important design objectives. The M2114A is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

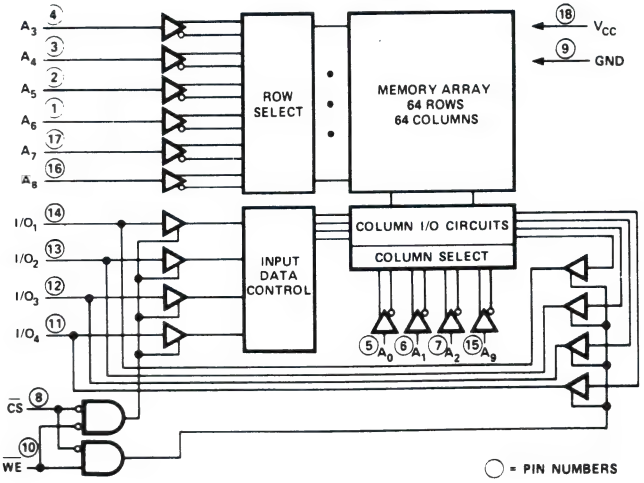
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
I/O_1–I/O_4	DATA INPUT/OUTPUT		

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -65°C to 135°C
Storage Temperature..... -65°C to 150°C
Voltage on any Pin
With Respect to Ground..... -3.5V to +7V
Power Dissipation..... 1.0W
D.C. Output Current 5mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = -55°C to +125°C, V_{CC} = 5V ±10%, unless otherwise noted.

SYMBOL	PARAMETER	M2114AL-3/L-4 Min.	Typ.(1)	Max.	M2114A-4/-5 Min.	Typ.(1)	Max.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)			10			10	μA	V_{IN} = 0 to 5.5V
$\|I_{LO}\|$	I/O Leakage Current			10			10	μA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}
I_{CC}	Power Supply Current		25	50		50	70	mA	V_{CC} = max, $I_{I/O}$ = 0 mA, T_A = -55°C
V_{IL}	Input Low Voltage	-3.0		0.8	-3.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	2.1	9.0		2.1	9.0		mA	V_{OL} = 0.4V
I_{OH}	Output High Current	-1.0	-2.5		-1.0	-2.5		mA	V_{OH} = 2.4V
I_{OS}(2)	Output Short Circuit Current			40			40	mA	V_{OUT} = GND

NOTE: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Duration not to exceed 30 seconds.

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels..... 0.8 Volt to 2.0 Volt
Input Rise and Fall Times..... 10 nsec
Input and Output Timing Levels..... 1.5 Volts
Output Load ..... 1 TTL Gate and C_L = 100 pF

A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = 5V ±10%, unless otherwise noted.

READ CYCLE [1]

SYMBOL	PARAMETER	M2114AL-3 Min.	M2114AL-3 Max.	M2114A-4/L-4 Min.	M2114A-4/L-4 Max.	M2114A-5 Min.	M2114A-5 Max.	UNIT
t_{RC}	Read Cycle Time	150		200		250		ns
t_A	Access Time		150		200		250	ns
t_{CO}	Chip Selection to Output Valid		70		70		85	ns
t_{CX}	Chip Selection to Output Active	10		10		10		ns
t_{OTD}	Output 3-state from Deselection		40		50		60	ns
t_{OHA}	Output Hold from Address Change	15		15		15		ns

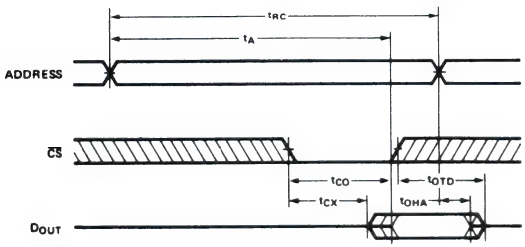
WRITE CYCLE [2]

SYMBOL	PARAMETER	M2114AL-3 Min.	M2114AL-3 Max.	M2114A-4/L-4 Min.	M2114A-4/L-4 Max.	M2114A-5 Min.	M2114A-5 Max.	UNIT
t_{WC}	Write Cycle Time	150		200		250		ns
t_W	Write Time	90		120		135		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTW}	Output 3-state from Write		40		50		60	ns
t_{DW}	Data to Write Time Overlap	90		120		135		ns
t_{DH}	Data Hold from Write Time	0		0		0		ns

NOTES:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

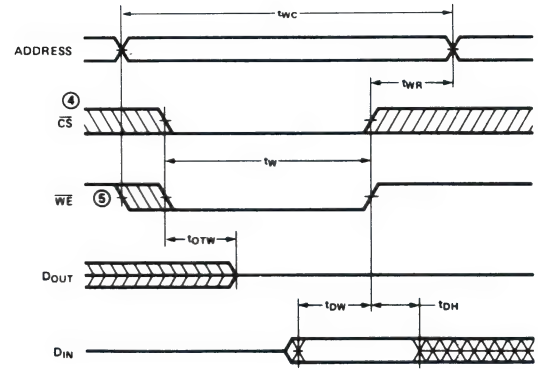
WAVEFORMS

READ CYCLE ③



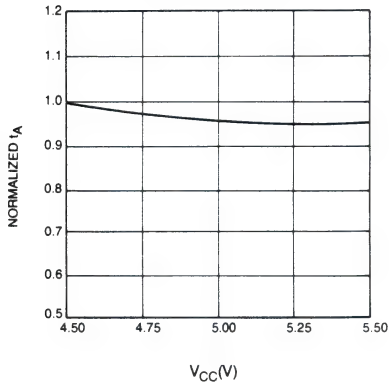
NOTES:
3. $\overline{WE}$ is high for a Read Cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition, the output buffers remain in a high impedance state.
5. $\overline{WE}$ must be high during all address transitions.

WRITE CYCLE

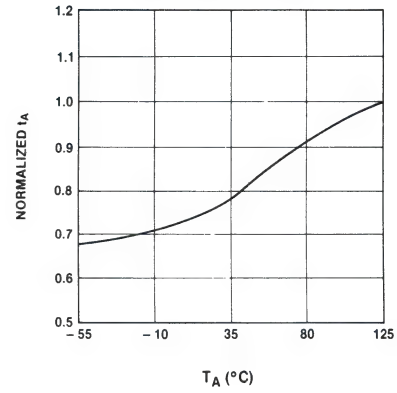


TYPICAL D.C. AND A.C. CHARACTERISTICS

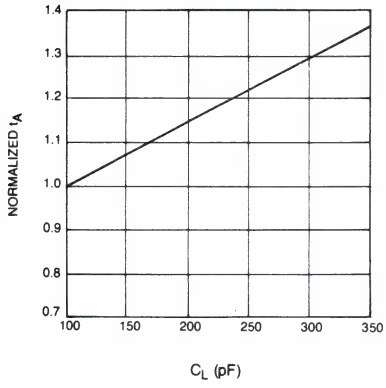
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



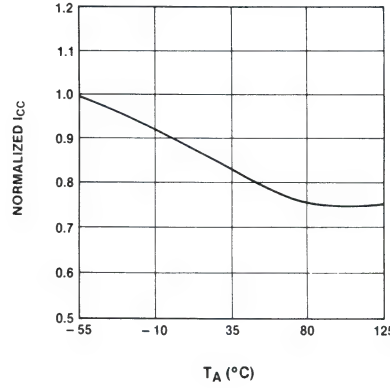
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



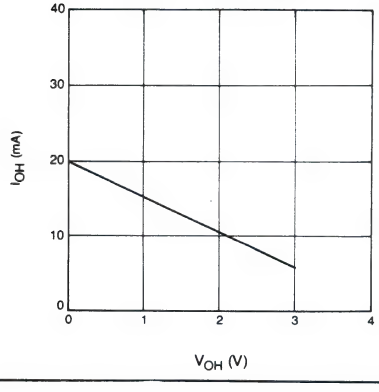
NORMALIZED ACCESS TIME VS. OUTPUT LOAD CAPACITANCE



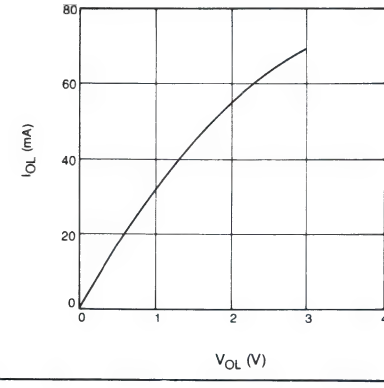
NORMALIZED POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



M2118 FAMILY
16,384 x 1 BIT DYNAMIC RAM

MILITARY

	M2118-4	M2118-7
Maximum Access Time (ns)	120	150
Read, Write Cycle (ns)	270	320
Read-Modify Cycle (ns)	320	410

- **Single +5V Supply, ±10% Tolerance**
- **HMOS Technology**
- **Low Power: 150 mW Max. Operating**
  11 mW Max. Standby
- **Low V_{DD} Current Transients**
- **All Inputs, Including Clocks, TTL Compatible**
- **$\overline{CAS}$ Controlled Output is Three-State, TTL Compatible**
- **$\overline{RAS}$ Only Refresh**
- **128 Refresh Cycles Required Every 2ms**
- **Allows Negative Overshoot V_{IL} min = −2V**
- **Military Temperature Range −55° to +85°C**

The Intel® M2118 is a 16,384 word by 1-bit Dynamic MOS RAM designed to operate from a single +5V power supply. The M2118 is fabricated using HMOS—a production proven process for high performance, high reliability, and high storage density.

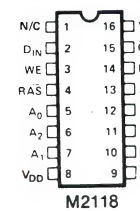
The M2118 uses a single transistor dynamic storage cell and advanced dynamic circuitry to achieve high speed with low power dissipation. The circuit design minimizes the current transients typical of dynamic RAM operation. These low current transients contribute to the high noise immunity of the M2118 in a system environment.

Multiplexing the 14 address bits into the 7 address input pins allows the M2118 to be packaged in the industry standard 16-pin DIP. The two 7-bit address words are latched into the M2118 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical timing requirements for $\overline{RAS}$ and $\overline{CAS}$ allow use of the address multiplexing technique while maintaining high performance.

The M2118 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is latched on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state.

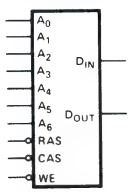
The single transistor storage cell requires refreshing for data retention. Refreshing is accomplished by performing $\overline{RAS}$-only refresh cycles, or normal read or write cycles on the 128 address combinations of A_0 through A_6 during a 2ms period. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

PIN CONFIGURATION



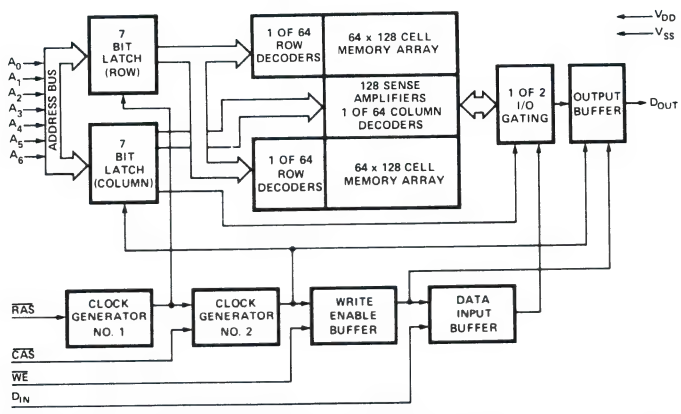
M2118

LOGIC SYMBOL



A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
$\overline{RAS}$	ROW ADDRESS STROBE
V_{DD}	POWER (+5V)
V_{SS}	GROUND

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .... −65°C to +95°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin Relative to V_{SS} 7.5V
Data Out Current 50mA
Power Dissipation 1.0W

*COMMENT:
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS [1]

T_A = −55°C to +85°C, V_{DD} = 5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits Min.	Typ.[2]	Max.	Unit	Test Conditions	Notes
$\|I_{LI}\|$	Input Load Current (any input)		0.1	10	µA	V_{IN}=V_{SS} to V_{DD}	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State		0.1	10	µA	Chip Deselected: $\overline{CAS}$ at V_{IH}, V_{OUT} = 0 to 5.5V	
I_{DD1}	V_{DD} Supply Current, Standby		1.2	2	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}	
I_{DD2}	V_{DD} Supply Current, Operating		21	25	mA	M2118-4, t_{RC} = t_{RCMIN}	3
			19	23	mA	M2118-7, t_{RC} = t_{RCMIN}	3
I_{DD3}	V_{DD} Supply Current; $\overline{RAS}$-Only Cycle		14	16	mA	M2118-4, t_{RC} = t_{RCMIN}	3
			12	14	mA	M2118-7, t_{RC} = t_{RCMIN}	3
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled		2	4	mA	$\overline{CAS}$ at V_{IL}, $\overline{RAS}$ at V_{IH}	3
V_{IL}	Input Low Voltage (all inputs)	-2.0		0.8	V		
V_{IH}	Input High Voltage (all inputs)	2.4		7.0	V		
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2mA	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -5mA	

NOTES:
1. All voltages referenced to V_{SS}.
2. Typical values are for T_A = 25°C and nominal supply voltages.
3. I_{DD} is dependent on output loading when the device output is selected. Specified $I_{DD\ MAX}$ is measured with the output open.

CAPACITANCE [1]

T_A = 25°C, V_{DD} = 5V ±10%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit
C_{I1}	Address, Data In	3	5	pF
C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, Data Out	4	7	pF

NOTES:
1. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:
$C = \frac{I\Delta t}{\Delta V}$ with ΔV equal to 3 volts and power supplies at nominal levels.

A.C. CHARACTERISTICS [1,2,3]

$T_A = -55°C$ to $+85°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

READ, WRITE, READ-MODIFY-WRITE AND REFRESH CYCLES

Symbol	Parameter	M2118-4 Min.	M2118-4 Max.	M2118-7 Min.	M2118-7 Max.	Unit	Notes
t_{RAC}	Access Time From $\overline{RAS}$		120		150	ns	4,5
t_{CAC}	Access Time From $\overline{CAS}$		65		80	ns	4,5,6
t_{REF}	Time Between Refresh		2		2	ms	
t_{RP}	$\overline{RAS}$ Precharge Time	120		135		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time(non-page cycles)	55		70		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	70	ns	7
t_{RSH}	$\overline{RAS}$ Hold Time	85		105		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	120		165		ns	
t_{ASR}	Row Address Set-Up Time	0		0		ns	
t_{RAH}	Row Address Hold Time	15		15		ns	
t_{ASC}	Column Address Set-Up Time	0		0		ns	
t_{CAH}	Column Address Hold Time	15		20		ns	
t_{AR}	Column Address Hold Time, to $\overline{RAS}$	70		90		ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{OFF}	Output Buffer Turn Off Delay	0	50	0	60	ns	

READ AND REFRESH CYCLES

t_{RC}	Random Read Cycle Time	270		320		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	140	10000	175	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	65	10000	95	10000	ns	
t_{RCS}	Read Command Set-Up Time	0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		ns	

WRITE CYCLE

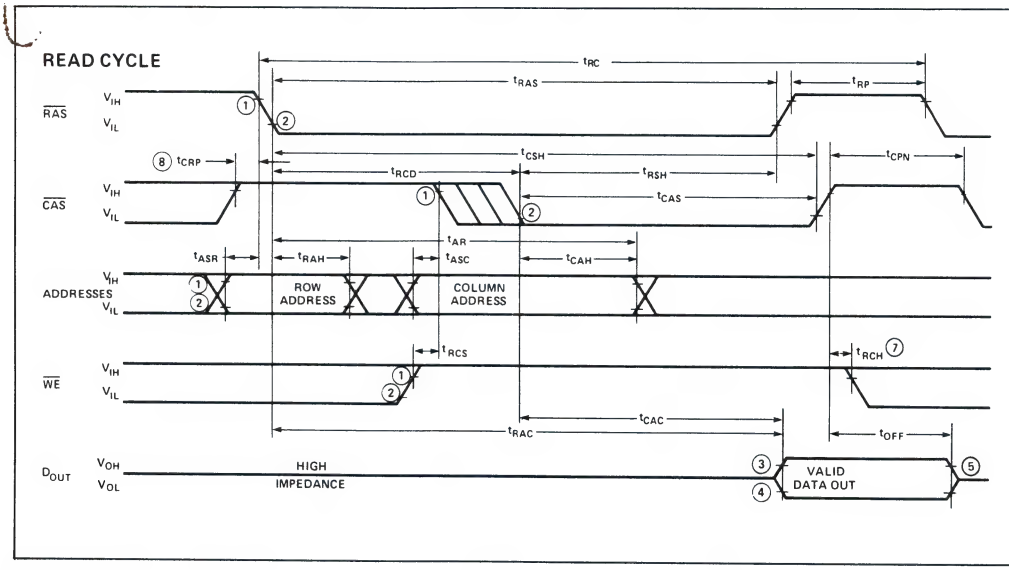
t_{RC}	Random Write Cycle Time	270		320		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	140	10000	175	10000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	65	10000	95	10000	ns	
t_{WCS}	Write Command Set-Up Time	0		0		ns	9
t_{WCH}	Write Command Hold Time	30		45		ns	
t_{WCR}	Write Command Hold Time, to $\overline{RAS}$	85		115		ns	
t_{WP}	Write Command Pulse Width	30		50		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	65		110		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	50		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		ns	
t_{DH}	Data-In Hold Time	30		45		ns	
t_{DHR}	Data-In Hold Time, to $\overline{RAS}$	85		115		ns	

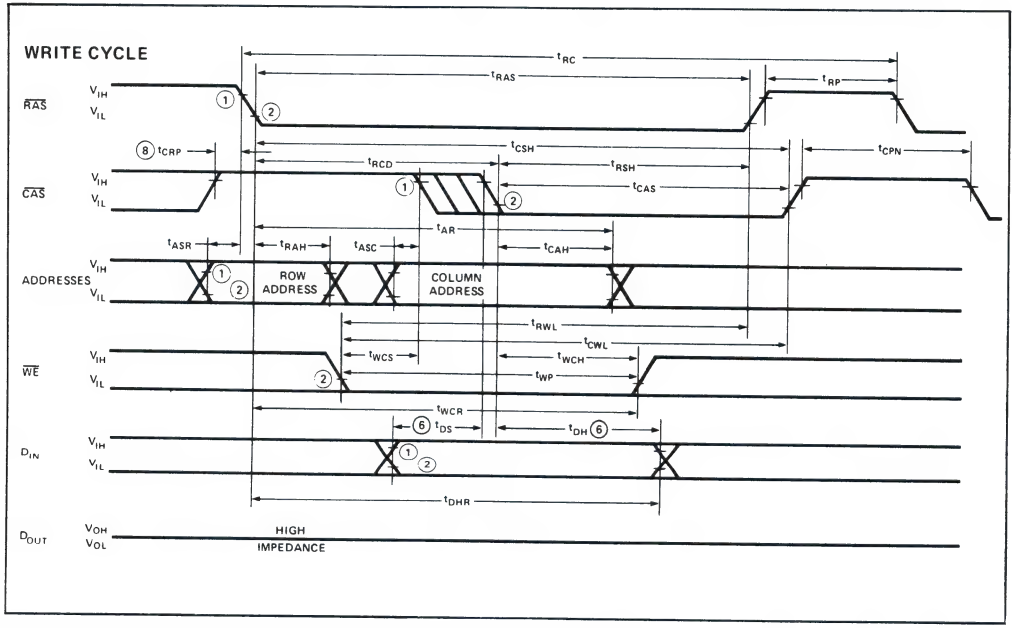
READ-MODIFY-WRITE CYCLE

t_{RWC}	Read-Modify-Write Cycle Time	320		410		ns	
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	190	10000	265	10000	ns	
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	120	10000	185	10000	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	120		150		ns	9
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	65		80		ns	9

NOTES:
1. All voltages referenced to V_{SS}.
2. Eight cycles are required after power up or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. A.C. Characteristics assume $t_T = 5ns$.
4. Assume that $t_{RCD} \leq t_{RCD}$(max). If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Load = 2 TTL loads and 100pF
6. Assumes $t_{RCD} \geq t_{RCD}$ (max.).
7. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is less than t_{RCD} (max.) access time is t_{RAC}. If t_{RCD} is greater than t_{RCD} (max.) access time is $t_{RCD} + t_{CAC}$.
8. t_T is measured between V_{IH} (min.) and V_{IL} (max.).
9. t_{WCS}, t_{CWD} and t_{RWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

WAVEFORMS

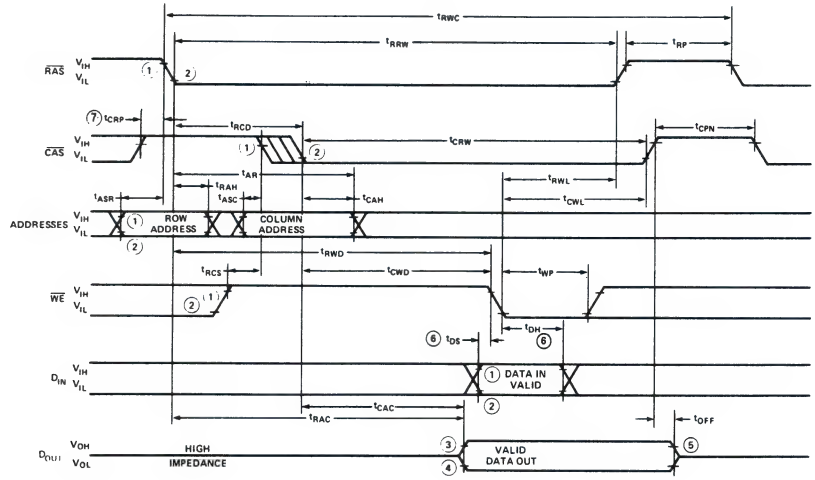




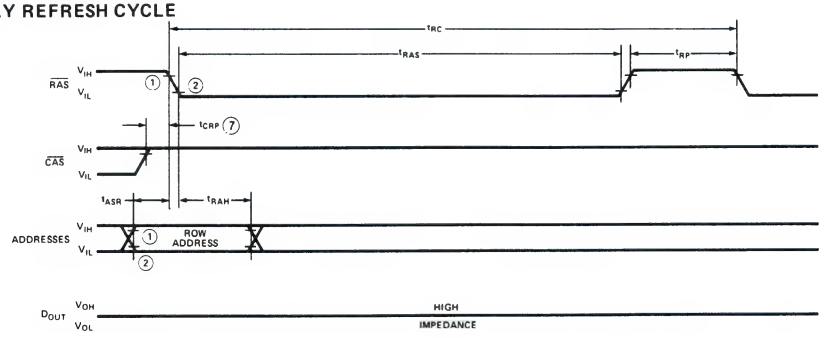
NOTES:
1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| < |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{RCH} IS REFERENCED TO THE TRAILING EDGE OF $\overline{CAS}$ OR $\overline{RAS}$, WHICHEVER OCCURS FIRST.
8. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

WAVEFORMS

READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



NOTES: 1,2. $V_{IH\ MIN}$ AND $V_{IL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS.
3,4. $V_{OH\ MIN}$ AND $V_{OL\ MAX}$ ARE REFERENCE LEVELS FOR MEASURING TIMING OF D_{OUT}.
5. t_{OFF} IS MEASURED TO $|I_{OUT}| \leq |I_{LO}|$.
6. t_{DS} AND t_{DH} ARE REFERENCED TO $\overline{CAS}$ OR $\overline{WE}$, WHICHEVER OCCURS LAST.
7. t_{CRP} REQUIREMENT IS ONLY APPLICABLE FOR $\overline{RAS}$/$\overline{CAS}$ CYCLES PRECEEDED BY A $\overline{CAS}$-ONLY CYCLE (i.e., FOR SYSTEMS WHERE $\overline{CAS}$ HAS NOT BEEN DECODED WITH $\overline{RAS}$).

M2147H
HIGH SPEED 4096 x 1 BIT STATIC RAM
MILITARY

	M2147H-3	M2147H
Max. Access Time (ns)	55	70
Max. Active Current (mA)	180	180
Max. Standby Current (mA)	30	30

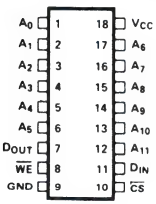
- **Pinout, Function, and Power Compatible to Industry Standard M2147**
- **HMOS II Technology**
- **Completely Static Memory—No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Direct Performance Upgrade for M2147**
- **Automatic Power-Down**
- **High Density 18-Pin Package**
- **Separate Data Input and Output**
- **Three-State Output**
- **Full Military Temperature Range −55°C to +125°C**

The Intel® M2147H is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS II, Intel's next generation high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high—deselecting the M2147H—the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

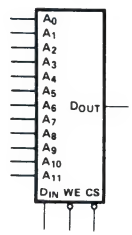
The M2147H is placed in an 18-pin package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

PIN CONFIGURATION

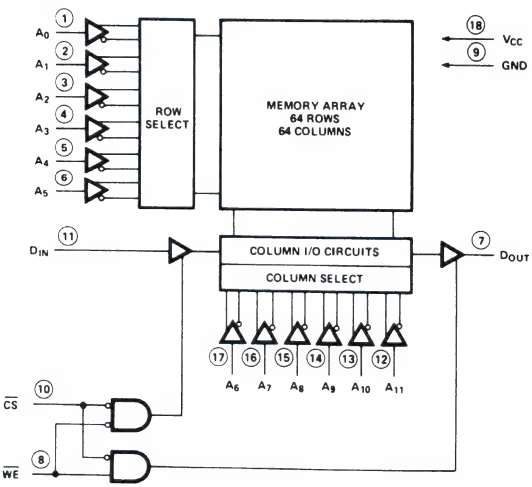


M2147H

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

April, 1980

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... −3.5V to +7V
Power Dissipation 1.2W
D.C. Output Current ..... 20 mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

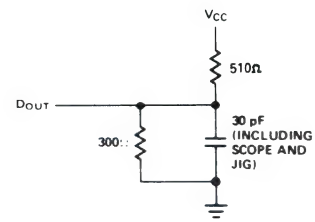
(T_A = −55°C to +125°C, V_{CC} = +5V ±10%, unless otherwise noted.)

Symbol	Parameter	M2147H-3, M2147H Min.	Typ.[2]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current (All Input Pins)		0.01	10	μA	V_{CC} = Max., V_{IN} = GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		0.1	50	μA	$\overline{CS}$ = V_{IH}, V_{CC} = Max., V_{OUT} = GND to 4.5V
I_{CC}	Operating Current		120	170	mA	T_A = 25°C; V_{CC} = Max., $\overline{CS}$ = V_{IL}, Outputs Open
				180	mA	T_A = −55°C; V_{CC} = Max., $\overline{CS}$ = V_{IL}, Outputs Open
I_{SB}	Standby Current		18	30	mA	V_{CC} = Min. to Max., $\overline{CS}$ = V_{IH}
I_{PO}[3]	Peak Power-On Current		35	70	mA	V_{CC} = GND to V_{CC} Min. $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	−3.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −4.0 mA
I_{OS}	Output Short Circuit Current	−200		+200	mA	V_{OUT} = GND to V_{CC}, T_A = −55°C

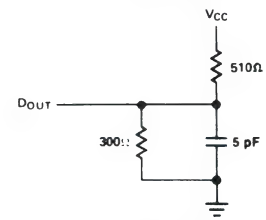
NOTES:
1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. Typical limits are at V_{CC} = 5V, T_A = +25°C, and Load A.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	0.8–2.0V
Output Load	See Load A



Load A



Load B

CAPACITANCE[4] (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	6	pF	V_{OUT} = 0V

NOTE:
4. This parameter is sampled and not 100% tested.

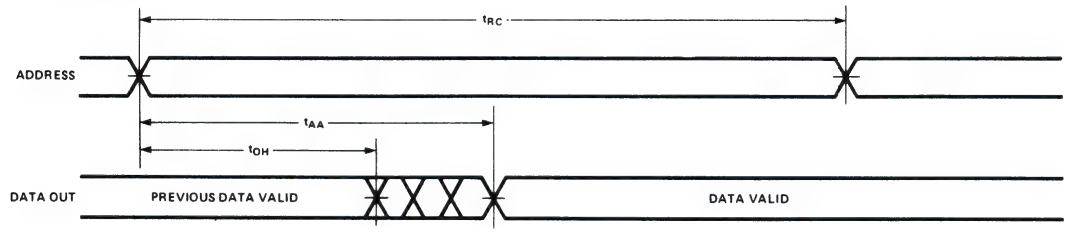
A.C. CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise noted.)

Read Cycle

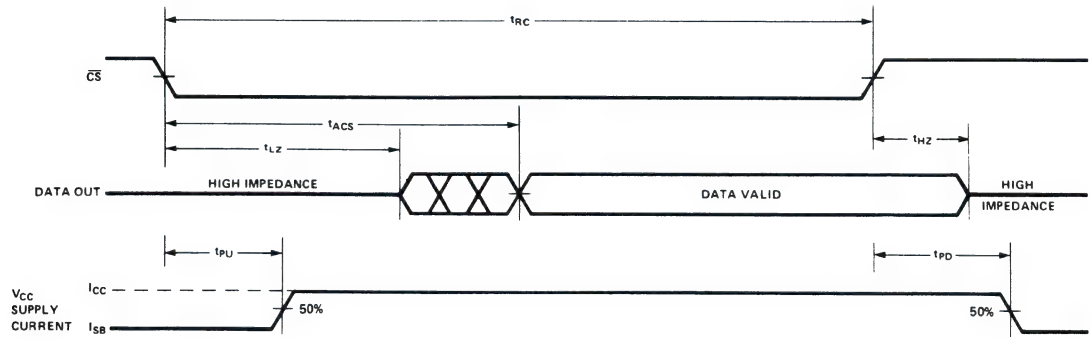
Symbol	Parameter	M2147H-3 Min.	M2147H-3 Max.	M2147H Min.	M2147H Max.	Unit	Test Conditions
t_{RC}[1]	Read Cycle Time	55		70		ns	
t_{AA}	Address Access Time		55		70	ns	
t_{ACS1}	Chip Select Access Time		55		70	ns	Note 8
t_{ACS2}	Chip Select Access Time		65		80	ns	Note 9
t_{OH}	Output Hold from Address Change	5		5		ns	
t_{LZ}[2,7]	Chip Selection to Output in Low Z	10		10		ns	Note 3
t_{HZ}[2,7]	Chip Deselection to Output in High Z	0	30	0	40	ns	Note 3
t_{PU}	Chip Selection to Power Up Time	0		0		ns	
t_{PD}	Chip Deselection to Power Down Time		20		30	ns	

WAVEFORMS

Read Cycle No. 1[4,5]



Read Cycle No. 2[4,6]

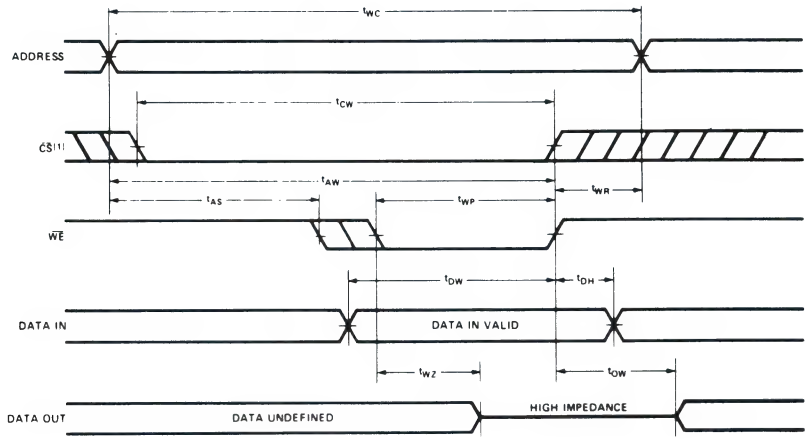


NOTES:
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with Load B.
4. $\overline{WE}$ is high for Read Cycles.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.
8. Chip deselected for greater than 55 ns prior to selection.
9. Chip deselected for a finite time that is less than 55 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1)

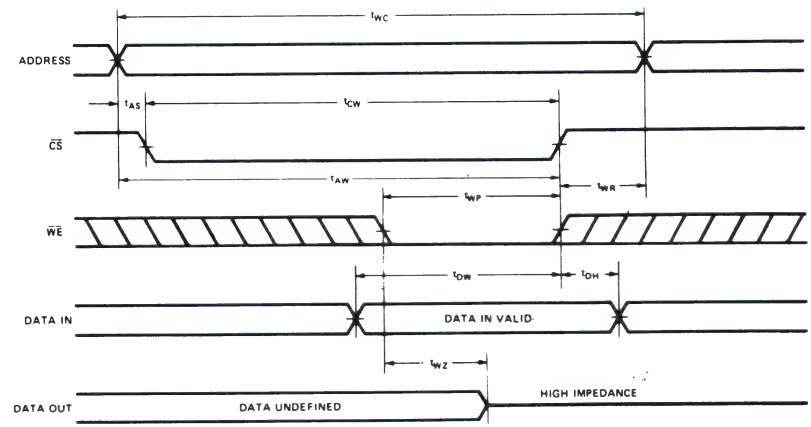
A.C. CHARACTERISTICS (Continued)
Write Cycle

Symbol	Parameter	M2147H-3 Min.	M2147H-3 Max.	M2147H Min.	M2147H Max.	Unit	Test Conditions
t_{WC}[2]	Write Cycle Time	55		70		ns	
t_{CW}	Chip Selection to End of Write	45		55		ns	
t_{AW}	Address Valid to End of Write	45		55		ns	
t_{AS}	Address Setup Time	0		0		ns	
t_{WP}	Write Pulse Width	25		40		ns	
t_{WR}	Write Recovery Time	10		15		ns	
t_{DW}	Data Valid to End of Write	25		30		ns	
t_{DH}	Data Hold Time	10		10		ns	
t_{WZ}	Write Enabled to Output in High Z	0	25	0	35	ns	Note 3
t_{OW}	Output Active from End of Write	0		0		ns	Note 3

WAVEFORMS
Write Cycle No. 1
($\overline{WE}$ CONTROLLED)[4]



Write Cycle No. 2
($\overline{CS}$ CONTROLLED)[4]



NOTES:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady state voltage with Load B.
4. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

PRELIMINARY

M2148H
HIGH SPEED 1024 x 4 BIT STATIC RAM

MILITARY

	M2148H
Max. Access Time (ns)	70
Max. Active Current (mA)	180
Max. Standby Current (mA)	30

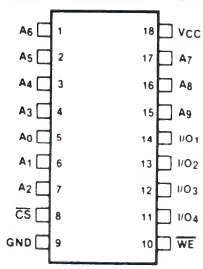
- HMOS II Technology
- Completely Static Memory—No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Single +5V Supply
- Automatic Power-Down
- High Density 18-Pin Package
- Industry Standard M2114A Pinout
- Common Data Input and Output
- Three-State Output
- Full Military Temperature Range −55°C to +125°C

The Intel® M2148H is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using HMOS II, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high—disabling the M2148H—the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are disabled.

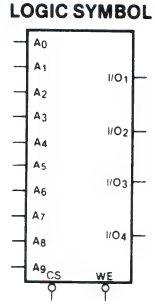
The M2148H is placed in an 18-pin package configured with the industry standard 1K x 4 pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data.

PIN CONFIGURATION



M2148H

LOGIC SYMBOL



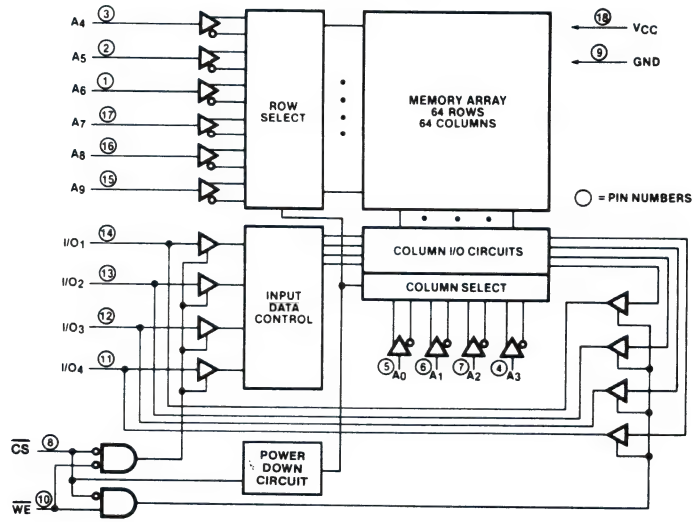
PIN NAMES

A_0-A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
$\overline{CS}$	CHIP SELECT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)
GND	GROUND

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... −3.5V to +7V
Power Dissipation 1.2W
D.C. Output Current ..... 20 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS[1]

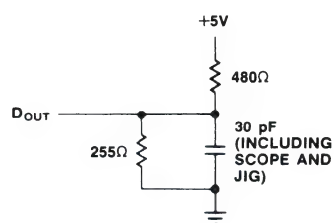
($T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise noted.)

Symbol	Parameter	M2148H Min.	M2148H Typ.[2]	M2148H Max.	Unit	Test Conditions
I_{LI}	Input Load Current (All Input Pins)		0.01	10	μA	V_{CC} = Max., V_{IN} = GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		0.1	50	μA	$\overline{CS} = V_H$, V_{CC} = Max., V_{OUT} = GND to 4.5V
I_{CC}	Operating Current		120	180	mA	$T_A = -55°C$; V_{CC} = Max., $\overline{CS} = V_{IL}$, Outputs Open
I_{SB}	Standby Current		15	30	mA	V_{CC} = Min. to Max., $\overline{CS} = V_{IH}$
I_{PO}[3]	Peak Power-On Current		25	50	mA	V_{CC} = GND to V_{CC} Min. $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	−3.0		0.8	V	
V_{IH}	Input High Voltage	2.1		6.0	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 8$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -4.0$ mA
I_{OS}[4]	Output Short Circuit Current		±200		mA	V_{OUT} = GND to V_{CC}

NOTES:
1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. Typical limits are at $V_{CC} = 5V$, $T_A = +25°C$, and Load A.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.
4. Duration not to exceed one second.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Load A

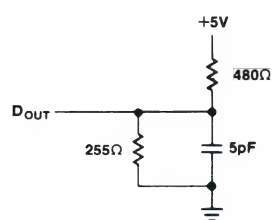


Load A

CAPACITANCE[4] ($T_A = 25°C$, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	5	pF	$V_{IN} = 0V$
$C_{I/O}$	Input/Output Capacitance	7	pF	$V_{I/O} = 0V$

NOTE:
4. This parameter is sampled and not 100% tested.



Load B

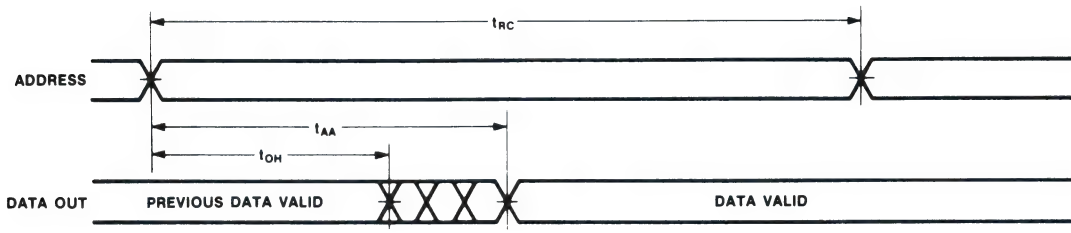
A.C. CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$ unless otherwise noted.)

Read Cycle

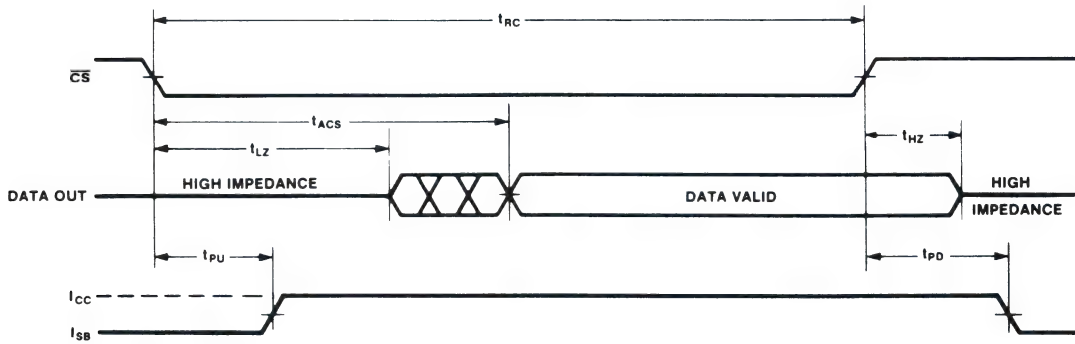
Symbol	Parameter	M2148H Min.	M2148H Max.	Unit	Test Conditions
t_{RC}	Read Cycle Time	70		ns	
t_{AA}	Address Access Time		70	ns	
t_{ACS1}	Chip Select Access Time		70	ns	Note 1
t_{ACS2}	Chip Select Access Time		80	ns	Note 2
t_{OH}	Output Hold from Address Change	5		ns	
t_{LZ}	Chip Selection Output in Low Z	20		ns	Note 6
t_{HZ}	Chip Deselection to Output in High Z	0	20	ns	Note 6
t_{PU}	Chip Selection to Power Up Time	0		ns	
t_{PD}	Chip Deselection to Power Down Time		30	ns	

WAVEFORMS

Read Cycle No. 1[3,4]



Read Cycle No. 2[3,5]



NOTES:
1. Chip deselected for greater than 55 ns prior to $\overline{CS}$ transition low.
2. Chip deselected for a finite time that is less than 55 ns prior to $\overline{CS}$ transition low. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)
3. $\overline{WE}$ is high for Read Cycles.
4. Device is continuously selected, $\overline{CS} = V_{IL}$.
5. Address valid prior to or coincident with $\overline{CS}$ transition low.
6. Transition is measured ± 500 mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

A.C. CHARACTERISTICS (Continued)

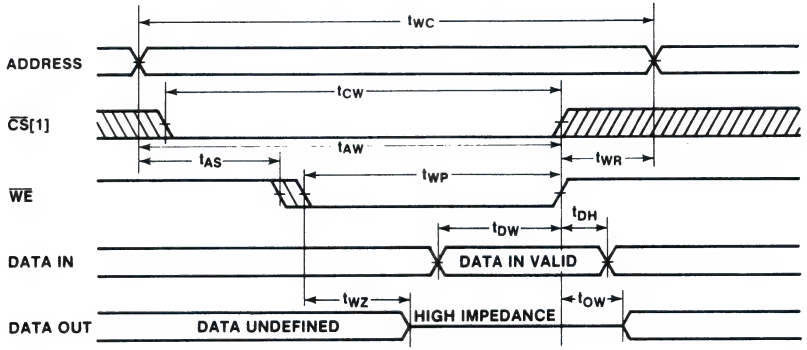
Write Cycle

Symbol	Parameter	M2148H Min.	M2148H Max.	Unit	Test Conditions
t_{WC}	Write Cycle Time	70		ns	
t_{CW}	Chip Selection to End of Write	65		ns	
t_{AW}	Address Valid to End of Write	65		ns	
t_{AS}	Address Setup Time	0		ns	
t_{WP}	Write Pulse Width	50		ns	
t_{WR}	Write Recovery Time	5		ns	
t_{DW}	Data Valid to End of Write	25		ns	
t_{DH}	Data Hold Time	0		ns	
t_{WZ}	Write Enabled to Output in High Z	0	25	ns	Note 2
t_{OW}	Output Active from End of Write	0		ns	Note 2

WAVEFORMS

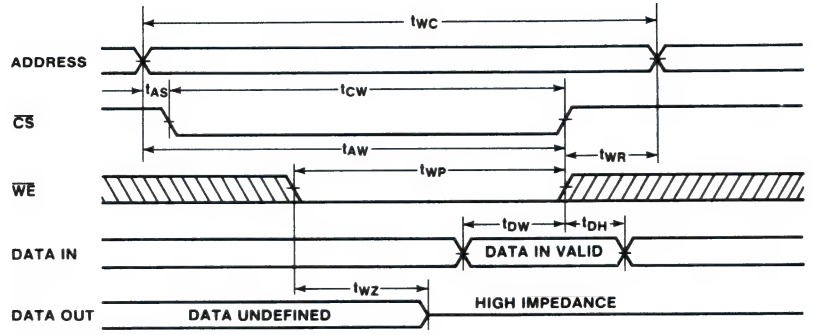
Write Cycle No. 1

($\overline{WE}$ CONTROLLED)



Write Cycle No. 2

($\overline{CS}$ CONTROLLED)



NOTES:
1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. Transition is measured ±500 mV from high impedance voltage with Load B. This parameter is sampled and not 100% tested.

M2716/M2716M
16K (2K x 8) UV ERASABLE PROM
MILITARY

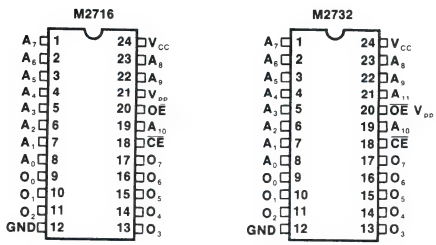
- **Military Temperature Range**
  M2716M: −55°C to 125°C
  M2716: −55°C to 100°C
- **5V ±10% V_{CC}**
- **Pin Compatible to Intel's M2732 32K EPROM**
- **Fast Access Time; 450 ns maximum**
- **Static Standby Mode**
- **Low Power Dissipation of 165 mW maximum standby power**
- **Inputs and Outputs TTL Compatible during Read and Program**

The Intel® M2716M and M2716 are 16 384-bit ultraviolet erasable and electrically programmable read only memories (EPROMs) specified over the military and extended temperature range respectively. They operate from a single +5V power supply, have a static power-down mode, and feature fast, single-address location programming. It makes designing with EPROMs faster, easier and more economical. Both products are manufactured from the same dice. Except for the operating temperature range, both products have the same electrical and programming specifications.

The M2716/M2716M has a static standby mode which reduces the power dissipation without increasing access time. The active power dissipation is reduced by over 60% in the standby power mode. Both are pin compatible to Intel's 32K military EPROM, the M2732.

The M2716/M2716M has the simplest and fastest method devised yet for programming EPROMs—single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the M2716's single-address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATIONS



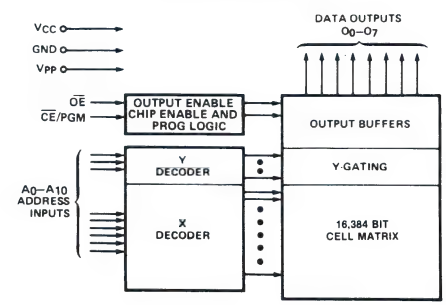
PIN NAMES

A_0–A_{10}	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0–O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section

Absolute Maximum Ratings*

Temperature Under Bias ..... −65°C to + 135°C
Storage Temperature ..... −65°C to + 150°C
All Input or Output Voltages with Respect to Ground ..... + 6V to − 0.3V
V_{PP} Supply Voltage with Respect to Ground During Program ..... + 26.5V to − 0.3V

*Notice:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND A.C. READ OPERATING CONDITIONS

	Temperature Range	V_{CC}	V_{PP}
M2716M	−55°C to + 125°C	5V ± 10%	V_{CC}
M2716	−55°C to + 100°C	5V ± 10%	V_{CC}

D.C. Characteristics

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ [3]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.5V
I_{PP1} [2]	V_{PP} Current			5	mA	V_{PP} = 5.5V
I_{CC1} [2]	V_{CC} Current (Standby)		10	30	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC2} [2]	V_{CC} Current (Active)		57	115	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage	− 0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = − 400 μA

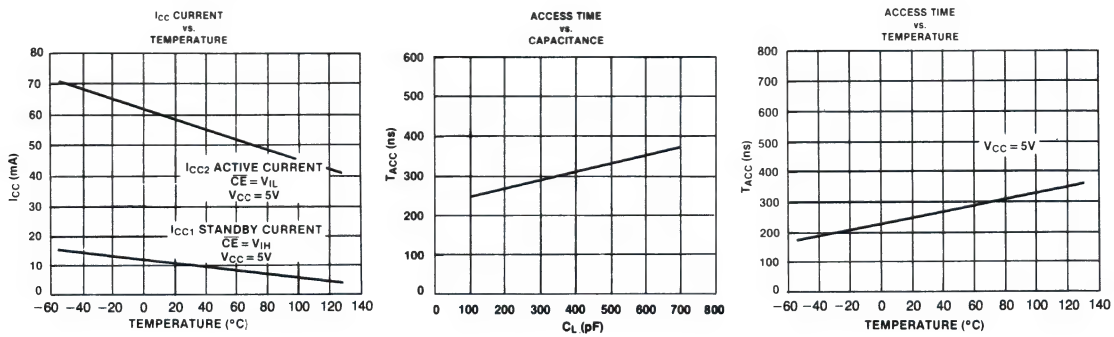
NOTES: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.

3. Typical values are for T_A = 25°C and nominal supply voltages.

4. This parameter is only sampled and is not 100% tested.

Typical Characteristics



A.C. Characteristics

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{ACC}	Address to Output Delay			450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay			450	ns	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay			150	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0		130	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold From Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

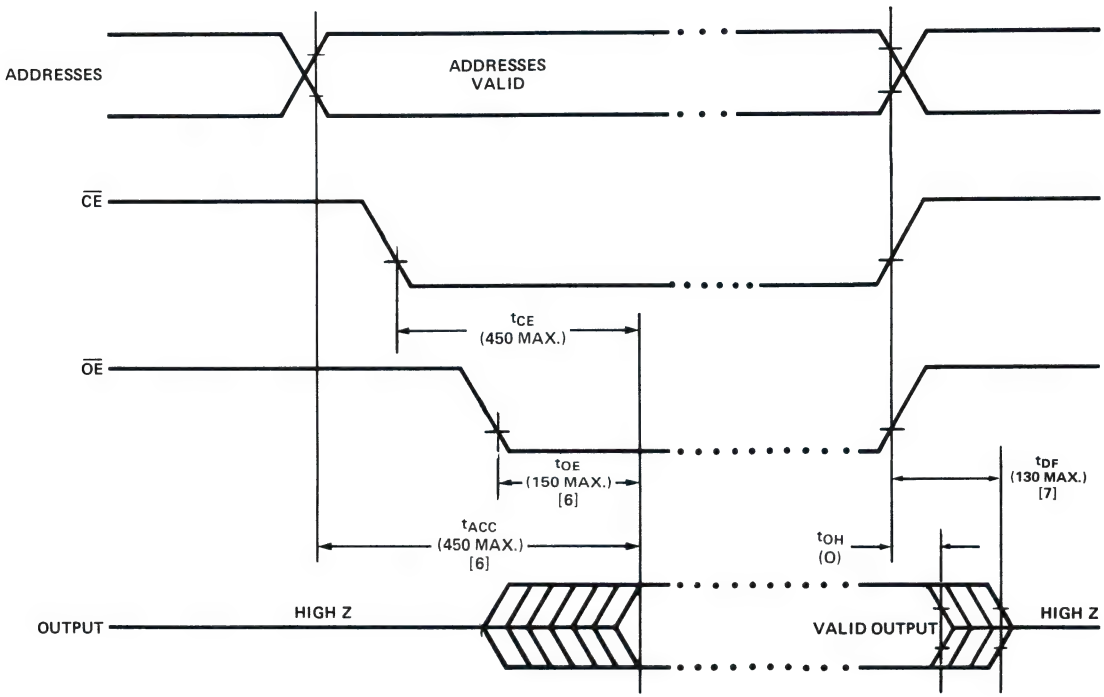
Capacitance[4] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions:

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms[5]



NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
5. All times shown in parentheses are minimum and are nsec unless otherwise specified.
6. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
7. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

DEVICE OPERATION

The five modes of operation of the M2716 are listed in Table 1. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

READ MODE

The M2716 has two control functions, both of which must be logically satisfied in order to obtain dat at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 150 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M2716 has a standby mode which reduces the active power dissipation by 75%, from 633 mW to 165 mW. The M2716 is placed in the standby mode by applying a TTL high special to the CE input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

OUTPUT OR-TIEING

Because M2716's are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connections. The two line control function allows for

a) the lowest possible memory power dissipation, and,
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING

Initially, and after each erasure, all bits of the M2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" wil be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec, active high, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can progam any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The M2716 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple M2716's in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled M2716's may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$ input programs the paralleled M2716's.

PROGRAM INHIBIT

Programming of multiple M2716's in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like units (including $\overline{OE}$) of the parallel M2716's may be common. A TTL level program pulse applied to a M2716's $\overline{CE}$ input with V_{PP} at 25V will program that M2716. A low level $\overline{CE}$ input inhibits the other M2716 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

DEVICE RELIABILITY

The M2716 is built on a proven 2 layer polysilicon NMOS technology. Extensive testing and monitoring has allowed us to achieve failure rates equal to other memory devices. For detailed failure rate predictions and reliability data, request Intel 2716 Reliability Report 19.

PRELIMINARY

M2732
32K (4K x 8) UV ERASABLE PROM
MILITARY

- **Military Temperature Range:**
  M2732: −55°C to +100°C
  M2732/S8416: −55°C to +125°C
- **Industry Standard Pinout . . . JEDEC Committee Approved**
- **Fast Access Time: 450 ns Maximum (M2732)**
- **5V ±10% V_{CC}**
- **Low Power Dissipation:**
  150 mA Max. Active Current
  45 mA Max. Standby Current
- **Pin Compatible to Intel® M2716 EPROM**
- **Three-State Output for Direct Bus Interface**

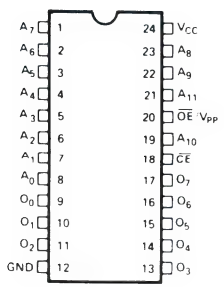
The Intel M2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The M2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control. The pinout is an industry standard and is compatible to the JEDEC committee approved pinouts for 16K to 64K bit EPROMs. This standardization, and with a 28-pin site design, allows easy upgrade to higher densities without changing board designs.

An important feature is the separate output control, Output Enable ($\overline{OE}$), from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

The M2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150 mA, while the maximum standby current is only 45 mA, a 70% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

The M2732/S8416 has the same electrical specifications as the M2732 but operation is over the military temperature range (−55°C to 125°C) at a 550 ns access time. It is ideal for applications which require a wider temperature range than the M2732 and high performance is not a requirement.

PIN CONFIGURATION



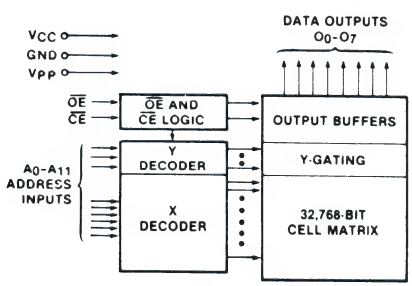
MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

BLOCK DIAGRAM



PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
All Input or Output Voltages with
Respect to Ground ..... +6V to -0.3V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND A.C. READ OPERATING CONDITIONS

	Temperature Range	V_{CC}
M2732	−55°C to +100°C	5V ±10%
M2732 S8416	−55°C to +125°C	5V ±10%

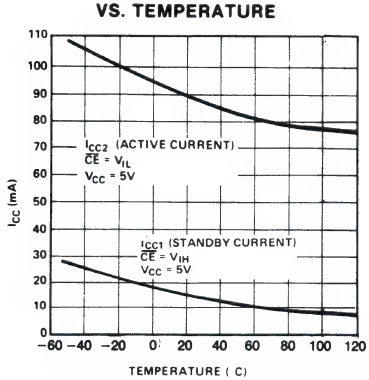
READ OPERATION

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
I_{LI1}	Input Load Current (except $\overline{OE}/V_{PP}$)			10	μA	$V_{IN} = 5.5V$
I_{LI2}	$\overline{OE}/V_{PP}$ Input Load Current			10	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.5V$
I_{CC1}	V_{CC} Current (Standby)		15	45	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
I_{CC2}	V_{CC} Current (Active)		85	150	mA	$\overline{OE} = \overline{CE} = V_{IL}$
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1mA$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400\mu A$

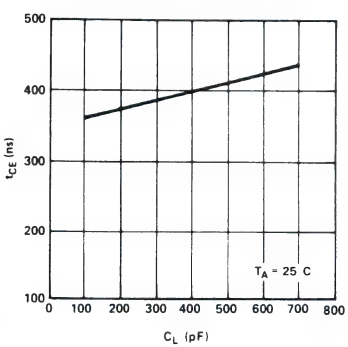
Note: 1. Typical values are for $T_A = 25°C$ and nominal supply voltages.

TYPICAL CHARACTERISTICS

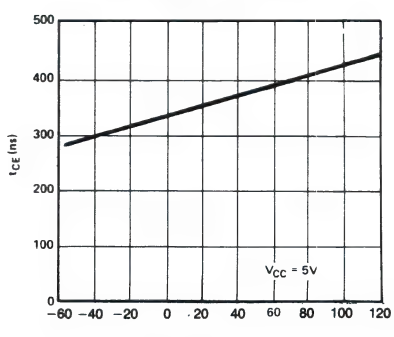
I_{CC} CURRENT VS. TEMPERATURE



$\overline{CE}$ TO OUTPUT DELAY (t_{CE}) VS. CAPACITANCE



$\overline{CE}$ TO OUTPUT DELAY (t_{CE}) VS. TEMPERATURE



A.C. CHARACTERISTICS

Symbol	Parameter		Limits Min.	Limits Typ.[1]	Limits Max.	Unit	Test Conditions
t_{ACC}	Address to Output Delay	M2732			450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
		M2732/S8416			550		
t_{CE}	$\overline{CE}$ to Output Delay	M2732			450	ns	$\overline{OE} = V_{IL}$
		M2732/S8416			550		
t_{OE}	Output Enable to Output Delay				150	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float		0		130	ns	$\overline{CE} = V_{IL}$
t_{OH}	Address to Output Hold		0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

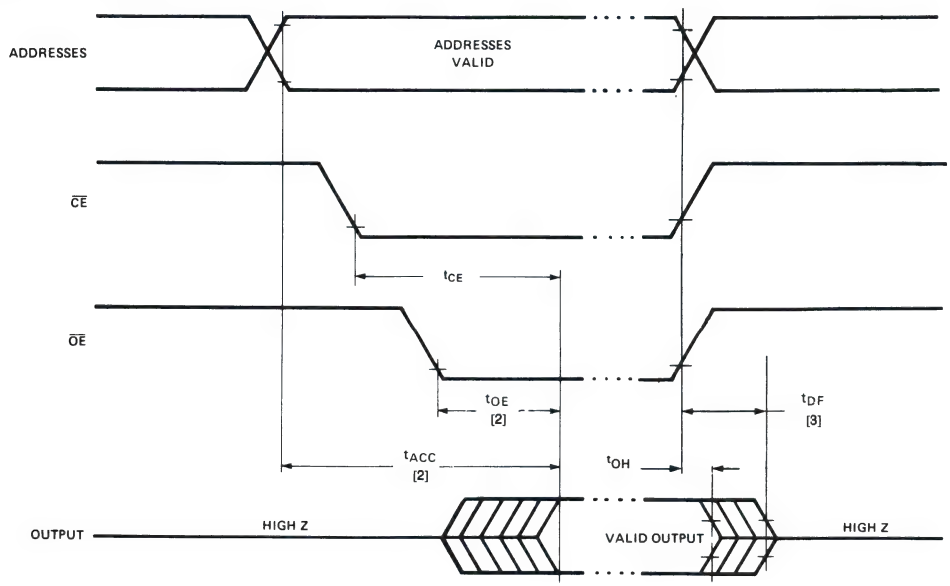
CAPACITANCE [1] $T_A = 25°C$, f = 1MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	$V_{IN} = 0V$
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance		12	pF	$V_{OUT} = 0V$

A.C. TEST CONDITIONS

Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. WAVEFORMS



NOTES:
1. THIS PARAMETER IS ONLY SAMPLED AND IS NOT 100% TESTED.
2. $\overline{OE}$ MAY BE DELAYED UP TO $t_{ACC} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{ACC}.
3. t_{DF} IS SPECIFIED FROM $\overline{OE}$ or $\overline{CE}$, WHICHEVER OCCURS FIRST.

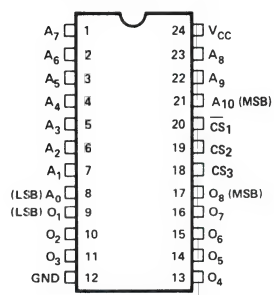
M3636
16K (2K x 8) BIPOLAR PROM

- −55°C to +125°C Operation
- Fast Access Time: 80ns Maximum
- Low Power Dissipation: 0.05mW/Bit Typically
- Three Chip Select Inputs for Easy Memory Expansion
- Pin Compatible to 8K PROMs
- Three-State Outputs
- Hermetic 24-Pin DIP
- Polycrystalline Silicon Fuses for Higher Fuse Reliability/Higher Programmability

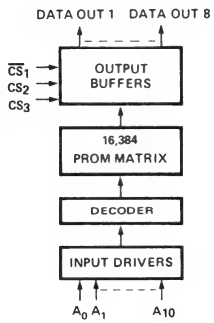
The Intel® M3636 is a fully decoded 16,384 bit PROM organized as 2048 words by 8 bits. The worst case access time of 80 ns is specified over the −55°C to +125°C temperature range and 5% V_{CC} power supply tolerances. There are three chip selects provided to facilitate expansion into larger PROM arrays. The PROMs use the Schottky clamped TTL technology with polycrystalline silicon fuses. All outputs are initially high and logic low levels can be electrically programmed in selected bit locations.

Prior to the 16,384 bit M3636, the highest density bipolar PROM available was 8196 bits. The high density of the M3636 now easily doubles the capacity without an increase in area on existing designs currently using 1024 by 8-bit PROMs. There is also little, if any, penalty in power since the power/bit is approximately one-half that of 8K PROMs. The M3636 is packaged in a hermetic 24-pin dual in-line package.

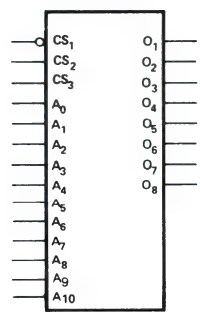
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

$A_0 - A_{10}$	ADDRESS INPUTS
$\overline{CS_1}$, CS_2, CS_3	CHIP SELECT INPUTS[1]
$O_1 - O_8$	DATA OUTPUTS

[1] To select the PROM $\overline{CS_1} = V_{IL}$ and $CS_2 = CS_3 = V_{IH}$

PROGRAMMING

The programming specifications are described in the PROM/ROM Programming section of the Data Catalog.

Absolute Maximum Ratings*

Temperature Under Bias ..... −65°C to +125°C
Storage Temperature ..... −65°C to +160°C
Output or Supply Voltages ..... −0.5V to 7 Volts
All Input Voltages ..... −1.5V to 5.5V
Output Currents 100mA

**COMMENT:* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

All Limits Apply for $V_{CC} = +5.0V \pm 5\%$, $T_A = -55°C$ to $125°C$ unless otherwise specified

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Unit	
I_{FA}	Address Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.25V$, $V_A = 0.45V$
I_{FS}	Chip Select Input Load Current		−0.05	−0.25	mA	$V_{CC} = 5.25V$, $V_S = 0.45V$
I_{RA}	Address Input Leakage Current			40	μA	$V_{CC} = 5.25V$, $V_A = 5.25V$
I_{RS}	Chip Select Input Leakage Current			40	μA	$V_{CC} = 5.25V$, $V_S = 5.25V$
$\|I_O\|$	Output Leakage for High Impedance State			60	μA	$V_O = 5.25V$ or 0.45V, $V_{CC} = 5.25V$, $CS_1 = 2.4V$
I_{SC}[1]	Output Short Circuit Current	−20	−35	−80	mA	$V_O = 0V$
V_{CA}	Address Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.75V$, $I_A = -10$ mA
V_{CS}	Chip Select Input Clamp Voltage		−0.9	−1.5	V	$V_{CC} = 4.75V$, $I_S = -10$ mA
V_{OH}	Output High Voltage	2.4	3.2V		V	$I_{OH} = -2.4$ mA, $V_{CC} = 4.75V$
V_{OL}	Output Low Voltage		0.3	0.45	V	$V_{CC} = 4.75V$, $I_{OL} = 10$ mA
I_{CC}	Power Supply Current		150	185	mA	$V_{CC} = 5.25V$
V_{IL}	Input "Low" Voltage			0.85	V	$V_{CC} = 5.0V \pm 5\%$, $T_A = 25°C$
V_{IH}	Input "High" Voltage	2.0			V	$V_{CC} = 5.0V \pm 5\%$, $T_A = 25°C$

Notes:
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. Unmeasured outputs are open during this test.

A.C. CHARACTERISTICS $V_{CC} = +5V \pm 10\%$, $T_A = -55°C$ to $125°C$

SYMBOL	PARAMETER	MAX. LIMITS	UNIT	CONDITIONS
T_A	Address to Output Delay	80	ns	$\overline{CS}_1 = V_{IL}$ and $CS_2 = CS_3 = V_{IH}$ to select the PROM.
t_{EN}	Output Enable Time	50	ns	
t_{DIS}	Output Disable Time	50	ns	

CAPACITANCE[1] $T_A = 25°C$, f = 1 MHz

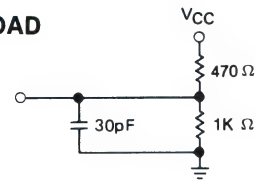
SYMBOL	PARAMETER	TYP. LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{INS}	Chip-Select Input Capacitance	6	10	pF	$V_{CC} = 5V$	$V_{IN} = 2.5V$
C_{OUT}	Output Capacitance	7	12	pF	$V_{CC} = 5V$	$V_{OUT} = 2.5V$

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

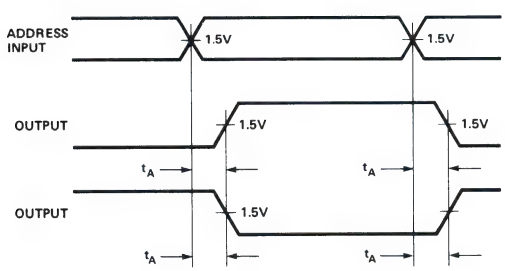
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 10 mA and 30 pF
Frequency of test – 2.5 MHz

10 mA TEST LOAD

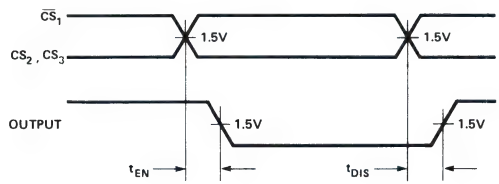


WAVEFORMS

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



Microcomputer Components 2

M8048/M8748/M8035L

SINGLE COMPONENT 8-BIT MICROCOMPUTER

MILITARY

*** 8048 Mask Programmable ROM**
*** 8748 User Programmable/Erasable EPROM**
*** 8035L Requires External ROM or EPROM**

- **-55°C to +125°C, 6 MHz Operation (M8048/M8035L)**
- **-55°C to +100°C, 3.6 MHz Operation (M8748)**
- **8-Bit CPU, ROM, RAM, I/O in Single Package**
- **Interchangeable ROM and EPROM Versions**
- **Single 5V Supply**
- **2.5 µsec and 5.0 µsec Cycle Versions All Instructions 1, or 2 Cycles.**
- **Over 90 Instructions: 70% Single Byte**
- **1K x 8 ROM/EPROM 64 x 8 RAM 27 I/O Lines**
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with 8080/8085 Series Peripherals**
- **Single Level Interrupt**

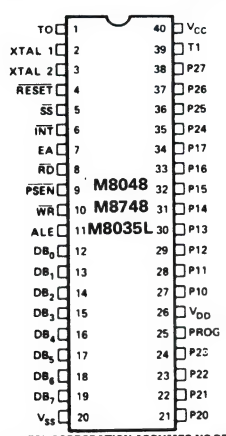
The Intel M8048/M8748/M8035L are totally self-sufficient 8-bit parallel computers fabricated on single silicon chips using Intel's N-Channel silicon gate MOS process.

The M8048 contains an 8-bit CPU, a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability, the M8048 can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The M8035L is the equivalent of an M8048 without program memory, and has the RAM power down mode of the M8048. To reduce development problems to a minimum and provide maximum flexibility, three interchangeable pin-compatible* versions of this single component microcomputer exist: the M8748 with user-programmable and erasable EPROM program memory for prototype and preproduction systems, the M8048 with factory-programmed mask ROM program memory for low cost, high volume production, and the M8035L without program memory for use with external program memories.

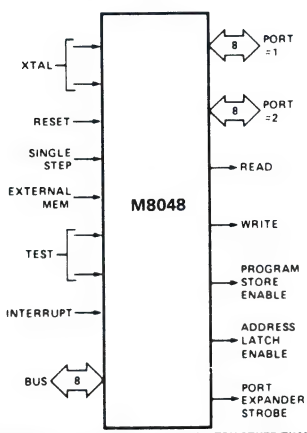
This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The M8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over 2 bytes in length.

*V_{DD} is used to program the M8748 and used for low power standby on the M8048/8035L.

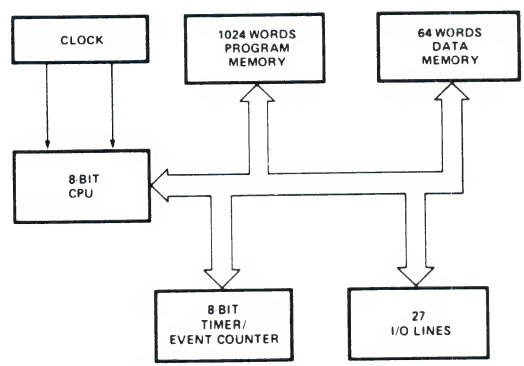
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Programming power supply; +25V during program, +5V during operation for both ROM and PROM. Low power standby pin in 8048 and 8035L.
V_{CC}	40	Main power supply; +5V during operation and programming.
PROG	25	Program pulse (+23V) input pin during 8748 programming. Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB_0-DB_7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENTO CLK instruction. T0 is also used during programming.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.

Designation	Pin#	Function
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down. (Active low) (Non TTL V_{IH})
$\overline{WR}$	10	Output strobe during a bus write. (Active low) Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in junction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle
Accumulator	ADD A, R	Add register to A	1	1
	ADD A, @R	Add data memory to A	1	1
	ADD A, #data	Add immediate to A	2	2
	ADDC A, R	Add register with carry	1	1
	ADDC A, @R	Add data memory with carry	1	1
	ADDC A, #data	Add immediate with carry	2	2
	ANL A, R	And register to A	1	1
	ANL A, @R	And data memory to A	1	1
	ANL A, #data	And immediate to A	2	2
	ORL A, R	Or register to A	1	1
	ORL A, @R	Or data memory to A	1	1
	ORL A, #data	Or immediate to A	2	2
	XRL A, R	Exclusive or register to A	1	1
	XRL A, @R	Exclusive or data memory to A	1	1
	XRL A, #data	Exclusive or immediate to A	2	2
	INC A	Increment A	1	1
	DEC A	Decrement A	1	1
	CLR A	Clear A	1	1
	CPL A	Complement A	1	1
	DA A	Decimal adjust A	1	1
	SWAP A	Swap nibbles of A	1	1
	RL A	Rotate A left	1	1
	RLC A	Rotate A left through carry	1	1
	RR A	Rotate A right	1	1
	RRC A	Rotate A right through carry	1	1
Input/Output	IN A, P	Input port to A	1	2
	OUTL P, A	Output A to port	1	2
	ANL P, #data	And immediate to port	2	2
	ORL P, #data	Or immediate to port	2	2
	INS A, BUS	Input BUS to A	1	2
	OUTL BUS, A	Output A to BUS	1	2
	ANL BUS, #data	And immediate to BUS	2	2
	ORL BUS, #data	Or immediate to BUS	2	2
	MOVD A, P	Input expander port to A	1	2
	MOVD P, A	Output A to expander port	1	2
	ANLD P, A	And A to expander port	1	2
	ORLD P, A	Or A to expander port	1	2
Registers	INC R	Increment register	1	1
	INC @R	Increment data memory	1	1
	DEC R	Decrement register	1	1
Branch	JMP addr	Jump unconditional	2	2
	JMPP @A	Jump indirect	1	2
	DJNZ R, addr	Decrement register and skip	2	2
	JC addr	Jump on carry = 1	2	2
	JNC addr	Jump on carry = 0	2	2
	JZ addr	Jump on A zero	2	2
	JNZ addr	Jump on A not zero	2	2
	JT0 addr	Jump on T0 = 1	2	2
	JNT0 addr	Jump on T0 = 0	2	2
	JT1 addr	Jump on T1 = 1	2	2
	JNT1 addr	Jump on T1 = 0	2	2
	JF0 addr	Jump on F0 = 1	2	2
	JF1 addr	Jump on F1 = 1	2	2
	JTF addr	Jump on timer flag	2	2
	JNI addr	Jump on $\overline{INT}$ = 0	2	2
	JBb addr	Jump on accumulator bit	2	2

	Mnemonic	Description	Bytes	Cycles
Subroutine	CALL addr	Jump to subroutine	2	2
	RET	Return	1	2
	RETR	Return and restore status	1	2
Flags	CLR C	Clear carry	1	1
	CPL C	Complement carry	1	1
	CLR F0	Clear flag 0	1	1
	CPL F0	Complement flag 0	1	1
	CLR F1	Clear flag 1	1	1
	CPL F1	Complement flag 1	1	1
Data Moves	MOV A, R	Move register to A	1	1
	MOV A, @R	Move data memory to a	1	1
	MOV A, #data	Move immediate to A	2	2
	MOV R, A	Move A to register	1	1
	MOV @R, A	Move A to data memory	1	1
	MOV R, #data	Move immediate to register	2	2
	MOV @R, #data	Move immediate to data memory	2	2
	MOV A, PSW	Move PSW to A	1	1
	MOV PSW, A	Move A to PSW	1	1
	XCH A, R	Exchange A and register	1	1
	XCHA, @R	Exchange A and data memory	1	1
	XCHD A, @R	Exchange nibble of A and register	1	1
	MOVX A, @R	Move external data memory to A	1	2
	MOVX @R, A	Move A to external data memory	1	2
	MOVP A, @A	Move to A from current page	1	2
	MOVP3 A, @A	Move to A from page 3	1	2
Timer/Counter	MOV A, T	Read timer/counter	1	1
	MOV T, A	Load timer/counter	1	1
	STRT T	Start timer	1	1
	STRT CNT	Start counter	1	1
	STOP TCNT	Stop timer/counter	1	1
	EN TCNTI	Enable timer/counter interrupt	1	1
	DIS TCNTI	Disable timer/counter interrupt	1	1
Control	EN I	Enable external interrupt	1	1
	DIS I	Disable external interrupt	1	1
	SEL RB0	Select register bank 0	1	1
	SEL RB1	Select register bank 1	1	1
	SEL MB0	Select memory bank 0	1	1
	SEL MB1	Select memory bank 1	1	1
	ENT0 CLK	Enable clock output on T0	1	1
	NOP	No operation	1	1

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias
- M8748 ..... -55° C to +100° C
- M8048/M8035L ..... -55° C to +125° C

Storage Temperature ..... -65° C to +150° C

Voltage On Any Pin With Respect to Ground ..... -0.5 to +7V

Power Dissipation ..... 1.5 Watt

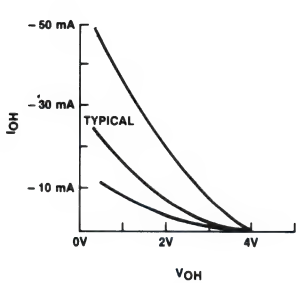
*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS

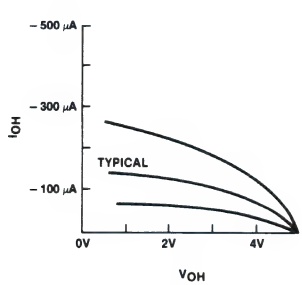
$T_A = -55°C$ to (100°C M8748/125°C M8048/M8035L), $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
V_{IL}	Input Low Voltage (All Except $\overline{RESET}$, X1, X2)	-.5		.7	V	
V_{IL1}	Input Low Voltage ($\overline{RESET}$, X1, X2)	-.5		.5	V	
V_{IH}	Input High Voltage (All Except XTAL1, XTAL 2, $\overline{RESET}$)	2.3		V_{CC}	V	
V_{IH1}	Input High Voltage ($\overline{RESET}$, X1, X2)	3.8		V_{CC}	V	
V_{OL}	Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)			.45	V	$I_{OL} = 1.2mA$
V_{OL1}	Output Low Voltage (All Other Outputs)			.45	V	$I_{OL} = 0.8mA$
V_{OH}	Output High Voltage (BUS)	2.4			V	$I_{OH} = -240\mu A$
V_{OH1}	Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	2.4			V	$I_{OH} = -50\mu A$
V_{OH2}	Output High Voltage (All Other Outputs)	2.4			V	$I_{OH} = -30\mu A$
I_{LI}	Input Leakage Current (T1, $\overline{INT}$)			± 10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{LI1}	Input Leakage Current (P10-P17, P20-P27, EA, $\overline{SS}$)			-700	μA	$V_{SS}+.45 \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current (BUS, TO) (High Impedance State)			± 10	μA	$V_{SS}+.45 \leq V_{IN} \leq V_{CC}$
I_{DD}	V_{DD} Supply Current		10	25	mA	
$I_{DD}+I_{CC}$	Total Supply Current		80	155	mA	

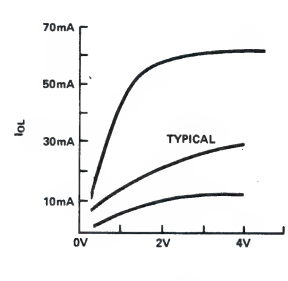
BUS



P1, P2

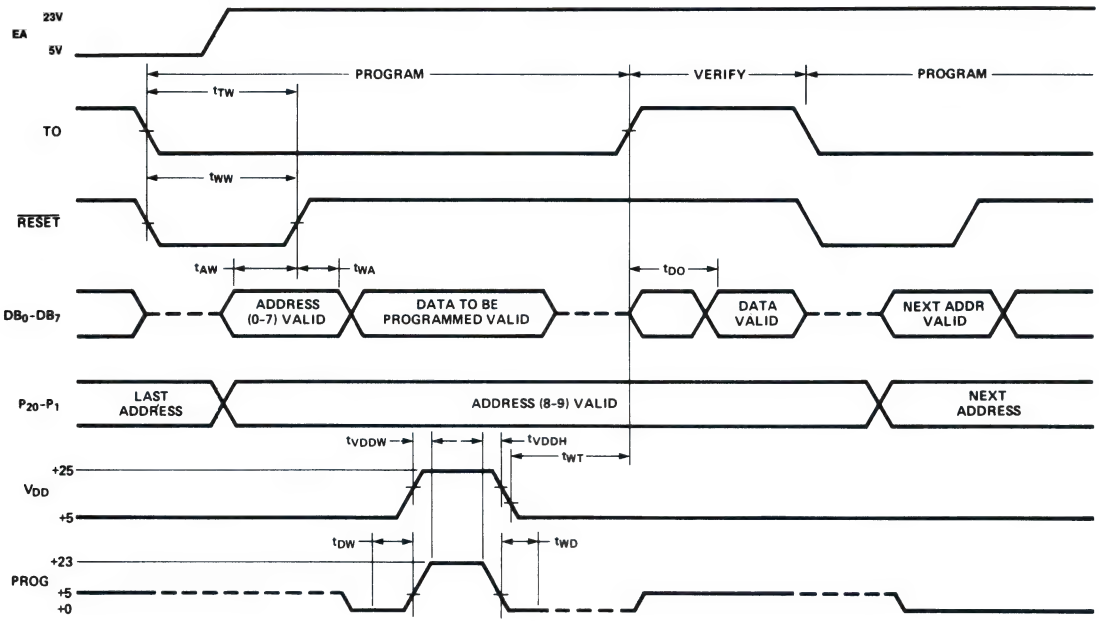


BUS, P1, P2

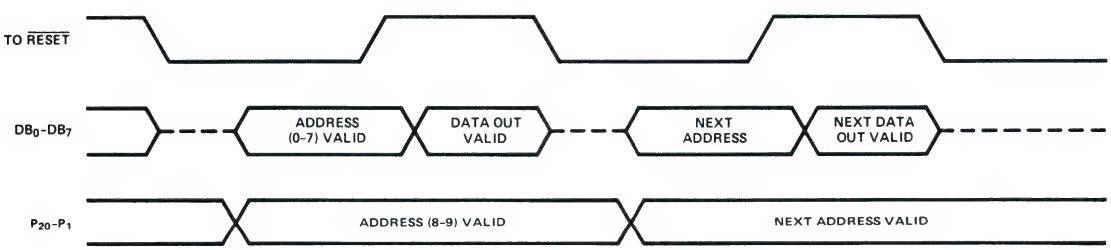


WAVEFORMS FOR PROGRAMMING

COMBINATION PROGRAM/VERIFY MODE (EPROM'S ONLY)



VERIFY MODE (ROM/EPROM)



NOTES:
1. PROG MUST FLOAT IF EA IS LOW (i.e., ≠23V), OR IF T0 = 5V FOR THE 8748. FOR THE 8048 PROG MUST ALWAYS FLOAT.
2. X_1 AND X_2 DRIVEN BY 3 MHz CLOCK WILL GIVE 5μsec t_{CY}. THIS IS ACCEPTABLE FOR ALL PARTS.

The 8748 EPROM can be programmed by either of two Intel products:

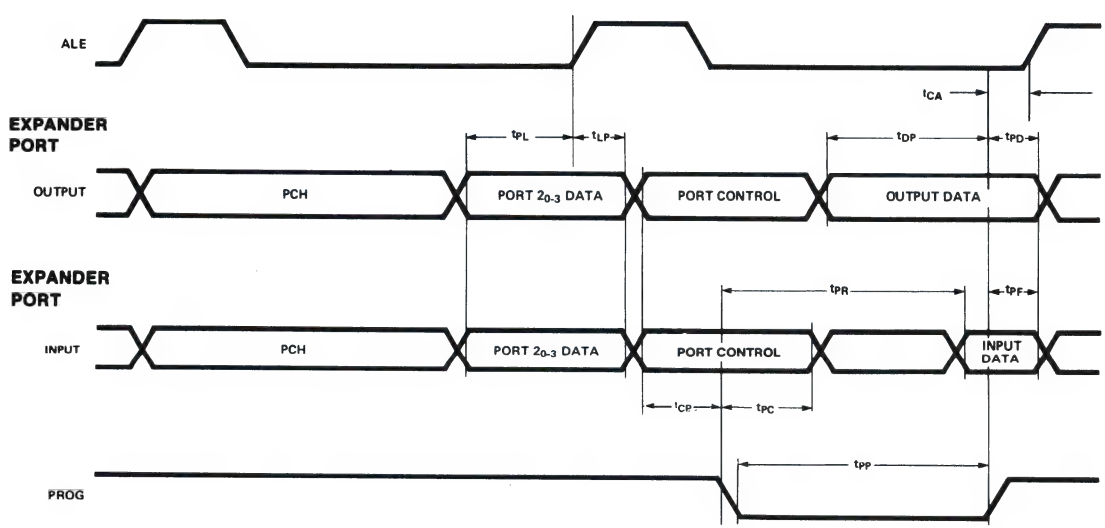
1. PROMPT-48 Microcomputer Design Aid, or
2. Universal PROM Programmer (UPP Series) peripheral of the Intellec® Development System with a UPP-848 Personality Card.

A.C. CHARACTERISTICS (PORT 2 TIMING)

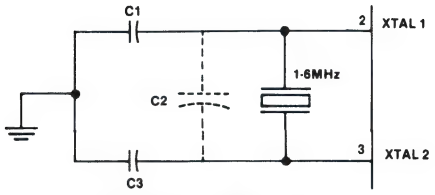
$T_A = 55°C$ to ($100°C$ M8748/$125°C$ M8048/M8035L), $V_{CC} = +5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CP}	Port Control Setup Before Falling Edge of $\overline{PROG}$	115		ns	
t_{PC}	Port Control Hold After Falling Edge of $\overline{PROG}$	65		ns	
t_{PR}	PROG to Time P2 Input Must Be Valid		860	ns	
t_{PF}	Input Data Hold Time	0	160	ns	
t_{DP}	Output Data Setup Time	230		ns	
t_{PD}	Output Data Hold Time	25		ns	
t_{PP}	$\overline{PROG}$ Pulse Width	920		ns	
t_{PL}	Port 2 I/O Data Setup	300		ns	
t_{LP}	Port 2 I/O Data Hold	120		ns	

PORT 2 TIMING



CRYSTAL OSCILLATOR MODE



C1 = 5pF ± ½pF + STRAY < 5pF
C2 = CRYSTAL + STRAY < 8pF
C3 = 20pF ± 1pF + STRAY < 5pF

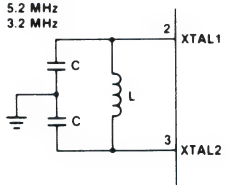
CRYSTAL SERIES RESISTANCE SHOULD BE LESS THAN 75Ω AT 6MHz; LESS THAN 180Ω AT 3.6MHz.

LC OSCILLATOR MODE

L	C	NOMINAL f
45 μH	20 pF	5.2 MHz
120 μH	20 pF	3.2 MHz

$$f \approx \frac{1}{2\pi\sqrt{LC'}}$$

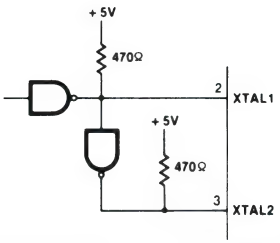
$$C' = \frac{C + 3C_{PP}}{2}$$



$C_{PP} \approx 5 - 10$ pF PIN-TO-PIN CAPACITANCE

EACH C SHOULD BE APPROXIMATELY 20 pF, INCLUDING STRAY CAPACITANCE.

DRIVING FROM EXTERNAL SOURCE



FOR XTAL 1 AND XTAL 2 DEFINE "HIGH" AS VOLTAGES ABOVE 1.6V AND "LOW" AS VOLTAGES BELOW 1.6V. THE DUTY CYCLE REQUIREMENTS FOR EXTERNALLY DRIVING XTAL 1 AND XTAL 2 USING THE CIRCUIT SHOWN ABOVE ARE AS FOLLOWS:

FOR THE 8048, XTAL 1 MUST BE HIGH 35-65% OF THE PERIOD AND XTAL 2 MUST BE HIGH 35-65% OF THE PERIOD.

FOR THE 8748, XTAL MUST BE HIGH 45-50% OF THE PERIOD AND XTAL 2 MUST BE HIGH 50-55% OF THE PERIOD.

RISE AND FALL TIMES MUST NOT EXCEED 20 ns.

PROGRAMMING, VERIFYING, AND ERASING THE 8748 EPROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

Pin	Function
XTAL 1	Clock Input (1 to 6MHz)
$\overline{\text{Reset}}$	Initialization and Address Latching
Test 0	Selection of Program or Verify Mode
EA	Activation of Program/Verify Modes
BUS	Address and Data Input Data Output During Verify
P20-1	Address Input
V_{DD}	Programming Power Supply
PROG	Program Pulse Input

WARNING:

An attempt to program a missocketed 8748 will result in severe damage to the part. An indication of a properly socketed part is the appearance of the ALE clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

1. V_{DD} = 5v, Clock applied or internal oscillator operating, $\overline{\text{RESET}}$ = 0v, TEST 0 = 5v, EA = 5v, BUS and PROG floating.
2. Insert 8748 in programming socket
3. TEST 0 = 0v (select program mode)
4. EA = 23V (activate program mode)
5. Address applied to BUS and P20-1
6. $\overline{\text{RESET}}$ = 5v (latch address)
7. Data applied to BUS
8. V_{DD} = 25v (programming power)
9. PROG = 0v followed by one 50ms pulse to 23V
10. V_{DD} = 5v
11. TEST 0 = 5v (verify mode)
12. Read and verify data on BUS
13. TEST 0 = 0v
14. $\overline{\text{RESET}}$ = 0v and repeat from step 5
15. Programmer should be at conditions of step 1 when 8748 is removed from socket.

AC TIMING SPECIFICATION FOR PROGRAMMING

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 25V \pm 1V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AW}	Address Setup Time to $\overline{RESET}$ ↑	4tcy			
t_{WA}	Address Hold Time After $\overline{RESET}$ ↑	4tcy			
t_{DW}	Data in Setup Time to PROG ↑	4tcy			
t_{WD}	Data in Hold Time After PROG ↓	4tcy			
t_{PH}	$\overline{RESET}$ Hold Time to Verify	4tcy			
t_{VDDW}	V_{DD}	4tcy			
t_{VDDH}	V_{DD} Hold Time After PROG ↓	0			
t_{PW}	Program Pulse Width	50	60	mS	
t_{TW}	Test 0 Setup Time for Program Mode	4tcy			
t_{WT}	Test 0 Hold Time After Program Mode	4tcy			
t_{DO}	Test 0 to Data Out Delay		4tcy		
t_{WW}	$\overline{RESET}$ Pulse Width to Latch Address	4tcy			
t_r, t_f	V_{DD} and PROG Rise and Fall Times	0.5	2.0	μs	
t_{CY}	CPU Operation Cycle Time	5.0		μs	
t_{RE}	$\overline{RESET}$ Setup Time Before EA ↓	4tcy			

Note: If Test 0 is high t_{DO} can be triggered by $\overline{RESET}$ ↓.

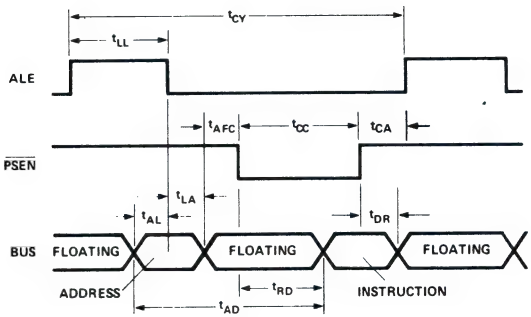
DC SPECIFICATION FOR PROGRAMMING

$T_A = 25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 25V \pm 1V$

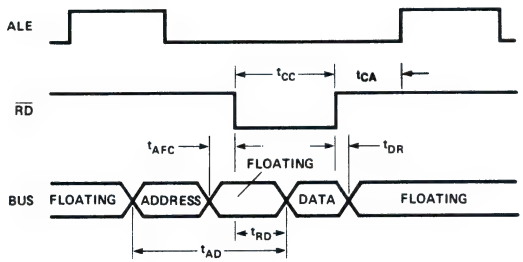
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DOH}	V_{DD} Program Voltage High Level	24.0	26.0	V	
V_{DDL}	V_{DD} Voltage Low Level	4.75	5.25	V	
V_{PH}	PROG Program Voltage High Level	21.5	24.5	V	
V_{PL}	PROG Voltage Low Level		0.2	V	
V_{EAH}	EA Program or Verify Voltage High Level	21.5	24.5	V	8748
V_{EAH1}	EA1 Verify Voltage High Level	11.4	12.6	V	8048
V_{EAL}	EA Voltage Low Level		5.25	V	
I_{DD}	V_{DD} High Voltage Supply Current		30.0	mA	
I_{PROG}	PROG High Voltage Supply Current		16.0	mA	
I_{EA}	EA High Voltage Supply Current		1.0	mA	

WAVEFORMS

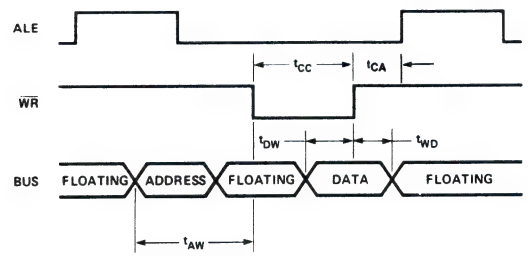
Instruction Fetch From External Program Memory



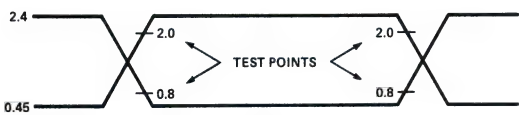
Read From External Data Memory



Write to External Data Memory



Input and Output Waveforms for A.C. Tests



A.C. CHARACTERISTICS

$T_A = -55°C$ to (100°C M8748/125°C M8048/M8035L), $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Symbol	Parameter	M8048 M8035L		M8748		Unit	Conditions (Note 1)
		Min.	Max.	Min.	Max.		
t_{LL}	ALE Pulse Width	200		300		ns	
t_{AL}	Address Setup to ALE	120		120		ns	
t_{LA}	Address Hold from ALE	80		80		ns	
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	400		600		ns	
t_{DW}	Data Setup before $\overline{WR}$	420		600		ns	
t_{WD}	Data Hold After $\overline{WR}$	80		120		ns	C_L = 20pF
t_{CY}	Cycle Time	2.5	15.0	4.17	15.0	μs	(3.6 MHz XTAL 8748)
t_{DR}	Data Hold	0	200	0	200	ns	
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In		400		600	ns	
t_{AW}	Address Setup to $\overline{WR}$	230		260		ns	
t_{AD}	Address Setup to Data In		600		900	ns	
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	-40		-60		ns	
t_{CA}	Control Pulse to ALE	10		10		ns	

Note 1: Control outputs: $C_L = 80$ pF $t_{CY} = 2.5\mu s$ for 8048/8035L
BUS Outputs: $C_L = 150$ pF $4.17\mu s$ for 8748

M8080A
8-BIT N-CHANNEL MICROPROCESSOR

The M8080A is functionally compatible with the Intel® 8080.

- **Fully Military Temperature Range −55°C to +125°C**
- **±10% Power Supply Tolerance**
- **2 μs Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **6 General Purpose Registers and an Accumulator**
- **16-Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **16-Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary, and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**

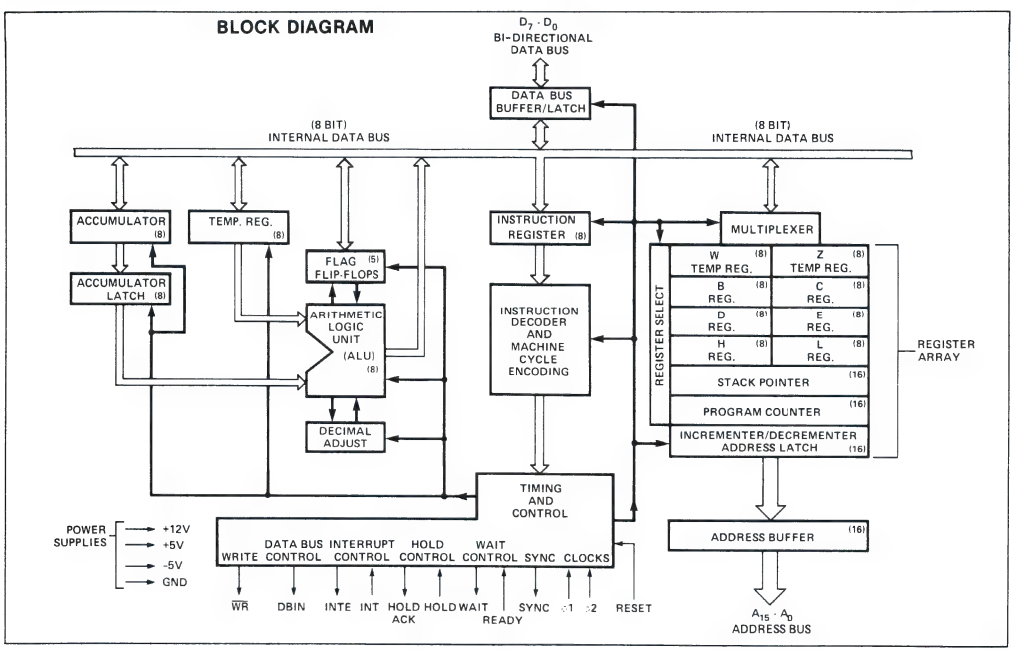
The Intel® M8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The M8080A contains 6 8-bit general purpose working registers and an accumulator. The 6 general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset 4 testable flags. A fifth flag provides decimal arithmetic operation.

The M8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store /retrieve the contents of the accumulator, flags, program counter and all of the 6 general purpose registers. The 16-bit stack pointer controls the addressing of this external stack. This stack gives the M8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bidirectional data busses are used to facilitate easy interface to memory and I/O. SIgnals to control the interface to memory and I/O are provided directly by the M8080A. Ultimate control of the address and data busses resides with the hold signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling device for (DMA) direct memory access or multi-processor operation.

BLOCK DIAGRAM



INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

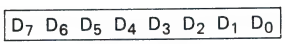
Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the M8080A. The ability to increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the M8080A instruction set.

The following special instruction group completes the M8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

Data and Instruction Formats

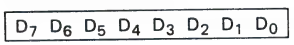
Data in the M8080A is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.



DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

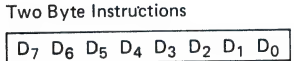


OP CODE

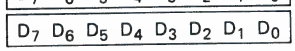
TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions

Two Byte Instructions



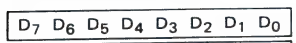
OP CODE



OPERAND

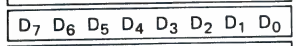
Immediate mode or I/O instructions

Three Byte Instructions

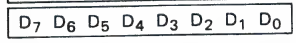


OP CODE

Jump, call or direct load and store instructions



LOW ADDRESS OR OPERAND 1



HIGH ADDRESS OR OPERAND 2

For the M8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.7W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	V_{SS}−1		V_{SS}+0.8	V	
V_{IHC}	Clock Input High Voltage	**8.5**		V_{DD}+1	V	
V_{IL}	Input Low Voltage	V_{SS}−1		V_{SS}+0.8	V	
V_{IH}	Input High Voltage	**3.0**		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs,
V_{OH}	Output High Voltage	3.7			V	I_{OH} = 150μA.
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		**50**	**80**	mA	Operation
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	**100**	mA	T_{CY} = .48 μsec
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leqslant V_{IN} \leqslant V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leqslant V_{CLOCK} \leqslant V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leqslant V_{IN} \leqslant V_{SS}$ +0.8V V_{SS} +0.8V $\leqslant V_{IN} \leqslant V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS}$ + 0.45V

CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = -5V

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:

1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

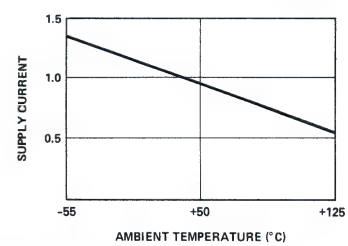


Figure 1. Typical Supply Current vs. Temperature, Normalized[3]

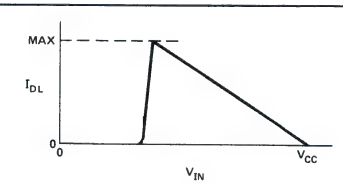


Figure 2. Data Bus Characteristic During DBIN

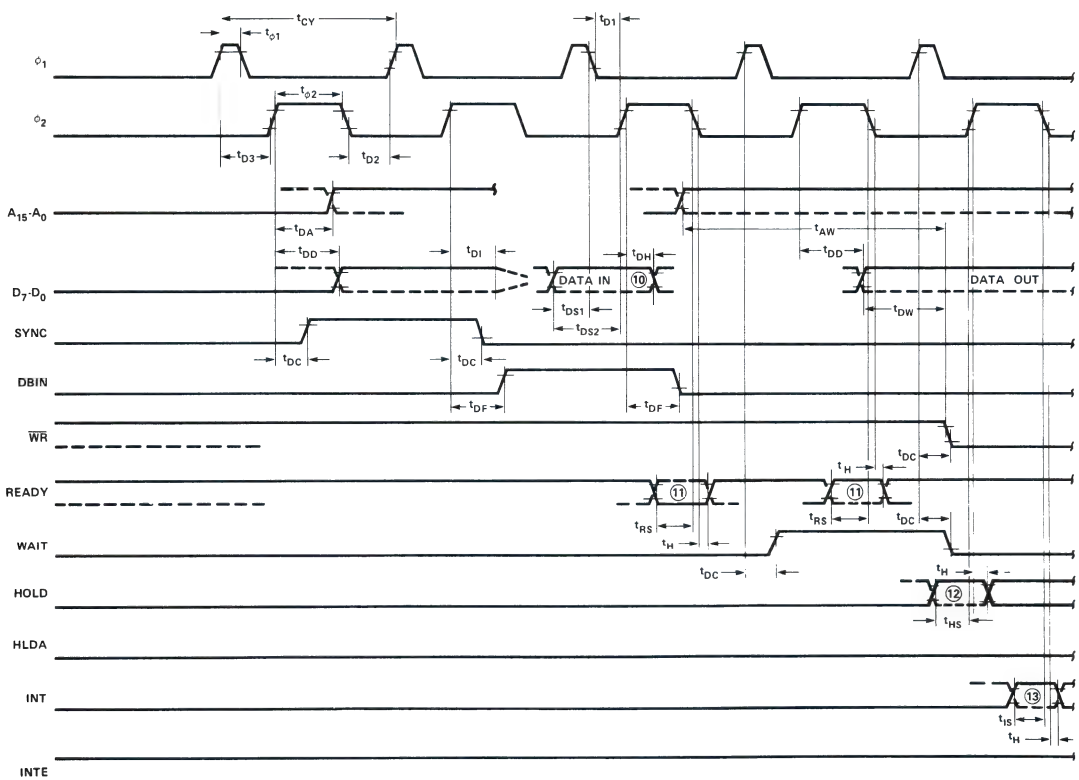
A.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{CY}[3]	Clock Period	0.48	2.0	μsec	
t_r, t_f	Clock Rise and Fall Time	0	50	nsec	
$t_{\phi 1}$	ϕ_1 Pulse Width	60		nsec	
$t_{\phi 2}$	ϕ_2 Pulse Width	220		nsec	
t_{D1}	Delay ϕ_1 to ϕ_2	0		nsec	
t_{D2}	Delay ϕ_2 to ϕ_1	80		nsec	
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	80		nsec	
t_{DA}[2]	Address Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{DD}[2]	Data Output Delay From ϕ_2		220	nsec	
t_{DC}[2]	Signal Output Delay From ϕ_1, or ϕ_2 (SYNC, $\overline{WR}$,WAIT,HLDA)		140	nsec	
t_{DF}[2]	DBIN Delay From ϕ_2	25	150	nsec	
t_{DI}[1]	Delay for Input Bus to Enter Input Mode		t_{DF}	nsec	
t_{DS1}	Data Setup Time During ϕ_1 and DBIN	30		nsec	

WAVEFORMS[14]

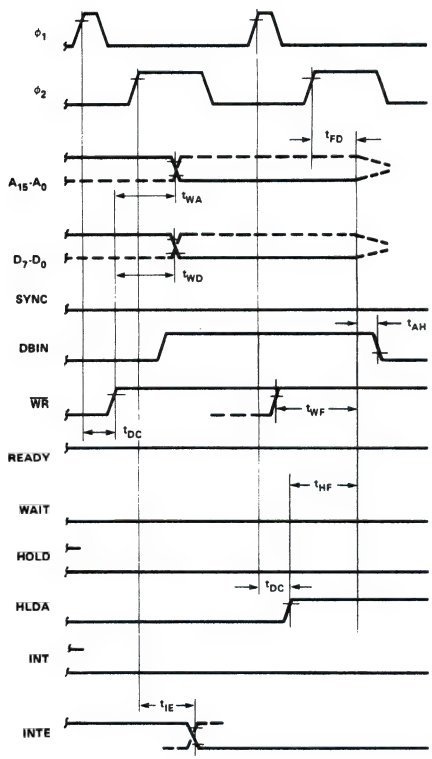
(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 7.0V, "0" = 1.0V; INPUTS "1" = 3.0V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



A.C. CHARACTERISTICS (Continued)

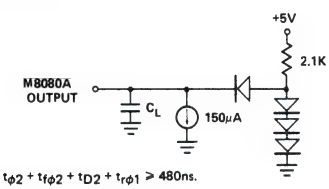
T_A = -55°C to +125°C, V_{DD} = +12V ±10%, V_{CC} = +5V ±10%, V_{BB} = -5V ±10%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Max.	Unit	Test Condition
t_{DS2}	Data Setup Time to ϕ_2 During DBIN	130		nsec	
t_{DH} [1]	Data Hold Time From ϕ_2 During DBIN	[1]		nsec	
t_{IE} [2]	INTE Output Delay From ϕ_2		200	nsec	C_L = 50pf
t_{RS}	READY Setup Time During ϕ_2	120		nsec	
t_{HS}	HOLD Setup Time to ϕ_2	140		nsec	
t_{IS}	INT Setup Time During ϕ_2	120		nsec	
t_H	Hold Time From ϕ_2 (READY, INT, HOLD)	0		nsec	
t_{FD}	Delay to Float During Hold (Address and Data Bus)		130	nsec	
t_{AW} [2]	Address Stable Prior to $\overline{WR}$	[5]		nsec	C_L = 50pf
t_{DW} [2]	Output Data Stable Prior to $\overline{WR}$	[6]		nsec	
t_{WD} [2]	Output Data Stable From $\overline{WR}$	[7]		nsec	
t_{WA} [2]	Address Stable From $\overline{WR}$	[7]		nsec	
t_{HF} [2]	HLDA to Float Delay	[8]		nsec	
t_{WF} [2]	$\overline{WR}$ to Float Delay	[9]		nsec	
t_{AH} [2]	Address Hold Time After DBIN During HLDA	-20		nsec	



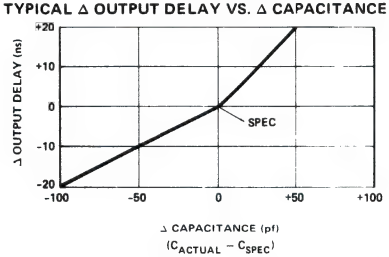
NOTES:

1. Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.
2. Load Circuit.



3. $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} \geq 480$ns.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



4. The following are relevant when interfacing the M8080A to devices having V_{IH} = 3.3V:
   a) Maximum output rise time from .8V to 3.3V = 100ns @ C_L = SPEC.
   b) Output delay when measured to 3.0V = SPEC +60ns @ C_L = SPEC.
   c) If $C_L \neq$ SPEC, add .6ns/pF if $C_L > C_{SPEC}$, subtract .3ns/pF (from modified delay) if $C_L < C_{SPEC}$.
5. $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi2} - 140$nsec.
6. $t_{DW} = t_{CY} - t_{D3} - t_{r\phi2} - 170$nsec.
7. If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.
8. $t_{HF} = t_{D3} + t_{r\phi2} - 50$ns.
9. $t_{WF} = t_{D3} + t_{r\phi2} - 10$ns
10. Data in must be stable for this period during DBIN - T_3. Both t_{DS1} and t_{DS2} must be satisfied.
11. Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
12. Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
13. Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)
14. This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

M8212
8-BIT INPUT/OUTPUT PORT

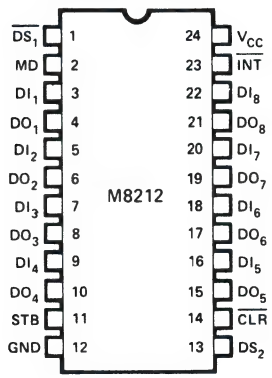
- **Fully Parallel 8-Bit Data Register and Buffer**
- **Service Request Flip-Flop for Interrupt Generation**
- **Low Input Load Current 0.25mA Max**
- **3-State Outputs**
- **Full Military Temperature Range -55°C to +125°C**
- **3.4V Output High Voltage for Direct Interface to M8080A CPU**
- **Asynchronous Register Clear**
- **Replaces Buffers, Latches, and Multiplexers in Microcomputer Systems**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**
- **24-Pin Dual In-Line Package**

The Intel® M8212/M3212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

*Note: The specifications for the M3212 are identical with those for the M8212.

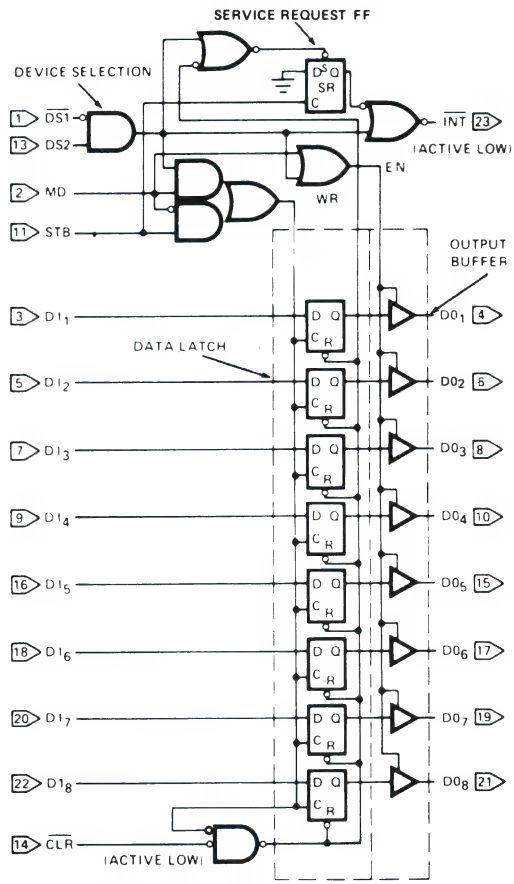
PIN CONFIGURATION



PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +160°C
All Output or Supply Voltages .... −0.5 to +7 Volts
All Input Voltages ..... −1.0 to 5.5 Volts
Output Currents ..... 100 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = -55°C to +125°C V_{CC} = +5V ±10%

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current STB, DS_2, CR, DI_1-DI_8 Inputs			−.25	mA	V_F = .45V
I_F	Input Load Current MD Input			−.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			−1.0	mA	V_F = .45V
I_R	Input Leakage Current STB, DS, CR, DI_1-DI_8 Inputs			10	μA	V_R = V_{CC}
I_R	Input Leakage Current MD Input			30	μA	V_R = V_{CC}
I_R	Input Leakage Current DS_1 Input			40	μA	V_R = V_{CC}
V_C	Input Forward Voltage Clamp			−1.2	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			.80	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 10mA
V_{OH}	Output "High" Voltage	3.5	4.0		V	I_{OH} = -.5mA
I_{OS}	Short Circuit Output Current	-15		-75	mA	V_{CC} = 5.0V
$\|I_O\|$	Output Leakage Current High Impedance State			20	μA	V_O = .45V to V_{CC}
I_{CC}	Power Supply Current		90	145	mA	

A.C. CHARACTERISTICS

T_A = -55°C to +125°C V_{CC} = +5V ±10%

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
t_{PW}	Pulse Width	40		ns	
t_{PD}	Data To Output Delay		30	ns	NOTE 1
t_{WE}	Write Enable To Output Delay		50	ns	NOTE 1
t_{SET}	Data Setup Time	20		ns	
t_H	Data Hold Time	30		ns	
t_R	Reset To Output Delay		55	ns	NOTE 1
t_S	Set To Output Delay		35	ns	NOTE 1
t_E	Output Enable/Disable Time		50	ns	NOTE 1 C_L = 30 pF
t_C	Clear To Output Delay		55	ns	NOTE 1

CAPACITANCE F = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = +5V, T_A = 25°C

Symbol	Test	LIMITS	
		Typ.	Max.
C_{IN}	$\overline{DS}_1$, MD Input Capacitance	9 pF	15 pF
C_{IN}	DS_2, $\overline{CLR}$, STB, DI_1-DI_8 Input Capacitance	5 pF	10 pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8 pF	15 pF

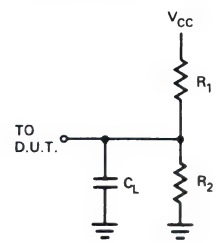
SWITCHING CHARACTERISTICS

Conditions of Test

Input Pulse Amplitude = 2.5V

Input Rise and Fall Times: 5 ns between 1V and 2V

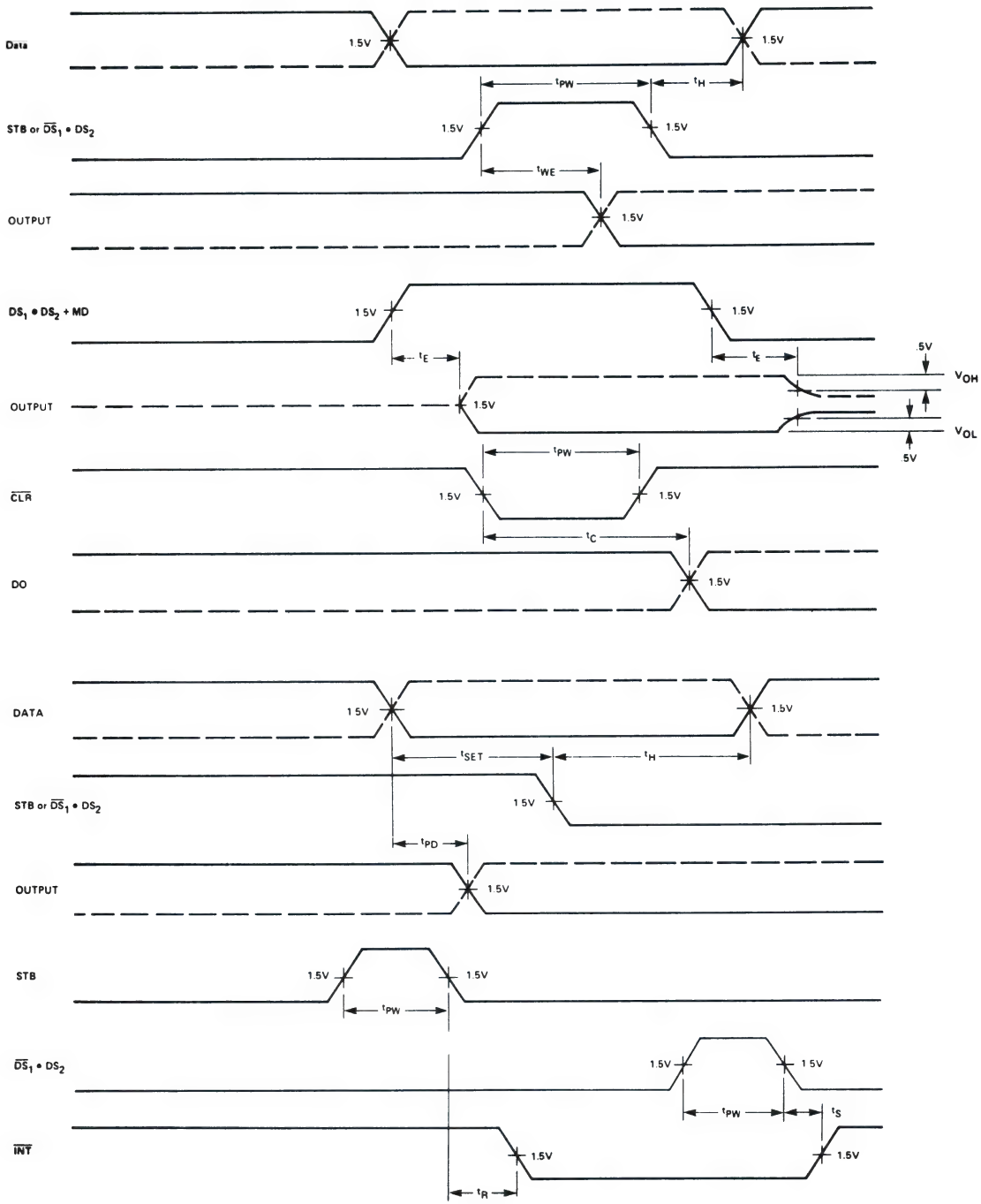
Test Load



NOTE 1:

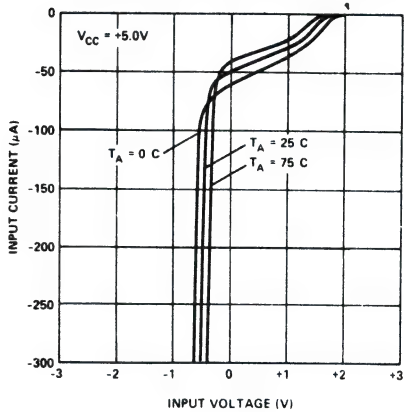
TEST	C_L	R_1	R_2
t_{PD}, t_{WE}, t_R, t_S, t_C	30pF	300Ω	600Ω
t_E, ENABLE↑	30pF	10KΩ	1KΩ
t_E, ENABLE↓	30pF	300Ω	600Ω
t_E, DISABLE↑	5pF	300Ω	600Ω
t_E, DISABLE↓	5pF	10KΩ	1KΩ

TIMING DIAGRAM

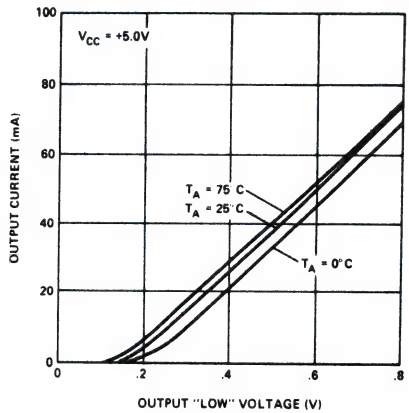


TYPICAL CHARACTERISTICS

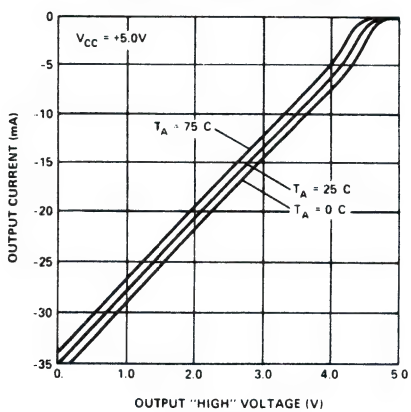
INPUT CURRENT VS. INPUT VOLTAGE



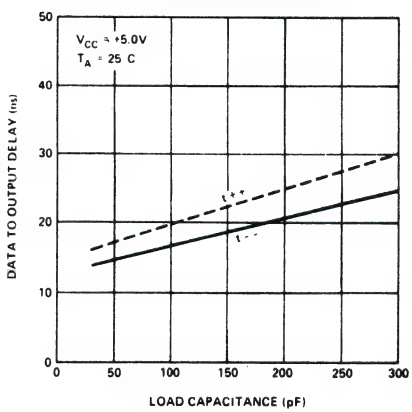
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



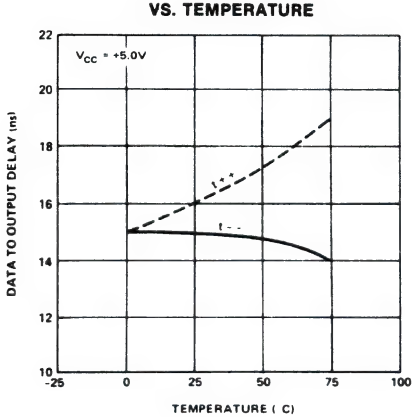
OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



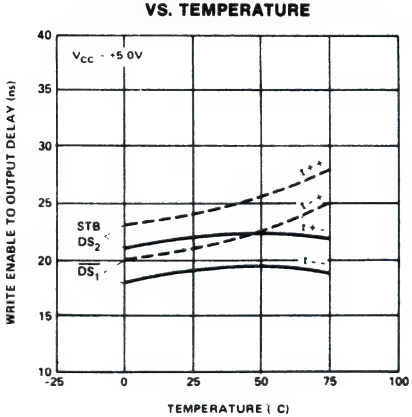
DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE



DATA TO OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE



M8214
PRIORITY INTERRUPT CONTROL UNIT

MILITARY TEMP.

- 8 Priority Levels
- Fully Expandable
- Current Status Register
- Priority Comparator
- 24-Pin Dual In-Line Package
- Full Military Temperature Range −55°C to +125°C
- +10% Power Supply Tolerance

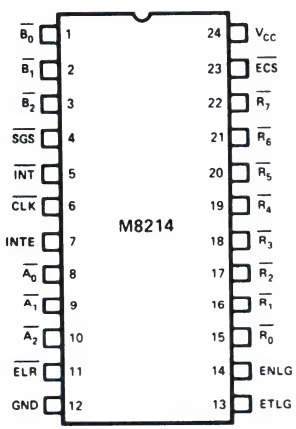
The Intel® M8214 is an 8-level priority interrupt control unit (PICU) designed to simplify interrupt-driven microcomputer systems.

The PICU can accept 8 requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue and interrupt to the system along with vector information to identify the service routine.

The M8214 is fully expandable by the use of open collector interrupt output vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt-driven microcomputer systems.

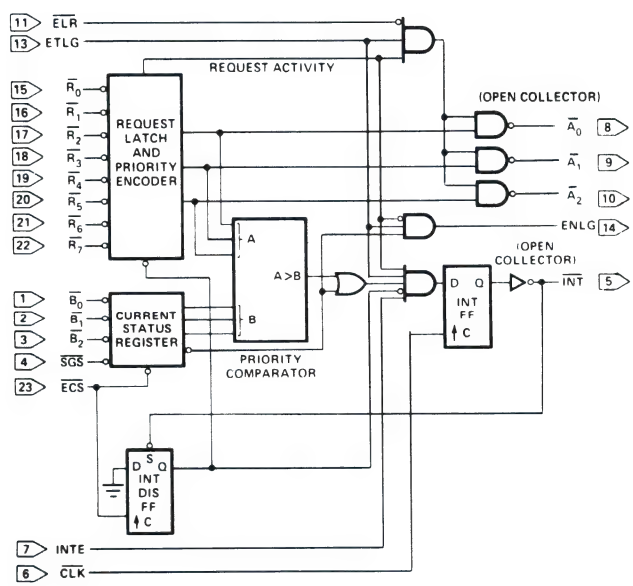
PIN CONFIGURATION



PIN NAMES

INPUTS		
$\overline{R_0}$-$\overline{R_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)	
$\overline{B_0}$-$\overline{B_2}$	CURRENT STATUS	
$\overline{SGS}$	STATUS GROUP SELECT	
$\overline{ECS}$	ENABLE CURRENT STATUS	
INTE	INTERRUPT ENABLE	
$\overline{CLK}$	CLOCK (INT F.F)	
$\overline{ELR}$	ENABLE LEVEL READ	
ETLG	ENABLE THIS LEVEL GROUP	
OUTPUTS		
$\overline{A_0}$-$\overline{A_2}$	REQUEST LEVELS	OPEN COLLECTOR
$\overline{INT}$	INTERRUPT (ACT. LOW)	OPEN COLLECTOR
ENLG	ENABLE NEXT LEVEL GROUP	

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +160°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Output Currents . . . . . 100 mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 55°C to 125°C V_{CC} = 5V ±10%

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage (all inputs)			-1.2	V	I_C=-5mA
I_F	Input Forward Current: ETLG input all other inputs		-.15 -.08	-0.5 -0.25	mA mA	V_F=0.45V
I_R	Input Reverse Current: ETLG input all other inputs			80 40	µA µA	V_R=5.5V
V_{IL}	Input LOW Voltage: all inputs			0.8	V	V_{CC}=5.0V
V_{IH}	Input HIGH Voltage: all inputs	2.0			V	V_{CC}=5.0V
I_{CC}	Power Supply Current		90	130	mA	See Note 2.
V_{OL}	Output LOW Voltage: all outputs		.3	.45	V	I_{OL}=10mA
V_{OH}	Output HIGH Voltage: ENLG output	2.4	3.0		V	I_{OH}=-1mA
I_{OS}	Short Circuit Output Current: ENLG output	-15	-35	-55	mA	V_{CC}=5.0V
I_{CEX}	Output Leakage Current: $\overline{INT}$, $\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$			100	µA	V_{CEX}=5.5V

NOTES:
1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.
2. B_0-B_2, $\overline{SGS}$, CLK, $\overline{R_0}$-$\overline{R_4}$ grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
t_{CY}	$\overline{CLK}$ Cycle Time	85			ns
t_{PW}	$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	25	15		ns
t_{ISS}	INTE Setup Time to $\overline{CLK}$	16	12		ns
t_{ISH}	INTE Hold Time after $\overline{CLK}$	20	10		ns
t_{ETCS}[2]	ETLG Setup Time to $\overline{CLK}$	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After $\overline{CLK}$	20	10		ns
t_{ECCS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	85	25		ns
t_{ECCH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{ECRS}[3]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	110	70		ns
t_{ECRH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			
t_{ECSS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	85	70		ns
t_{ECSH}[2]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{DCS}[2]	$\overline{SGS}$ and $\overline{B_0}$·$\overline{B_2}$ Setup Time to $\overline{CLK}$	90	50		ns
t_{DCH}[2]	$\overline{SGS}$ and $\overline{B_0}$·$\overline{B_2}$ Hold Time After $\overline{CLK}$	0			ns
t_{RCS}[3]	$\overline{R_0}$·$\overline{R_7}$ Setup Time to $\overline{CLK}$	100	55		ns
t_{RCH}[3]	$\overline{R_0}$·$\overline{R_7}$ Hold Time After $\overline{CLK}$	0			ns
t_{ICS}	$\overline{INT}$ Setup Time to $\overline{CLK}$	55	35		ns
t_{CI}	$\overline{CLK}$ to $\overline{INT}$ Propagation Delay		15	30	ns
t_{RIS}[4]	$\overline{R_0}$·$\overline{R_7}$ Setup Time to $\overline{INT}$	10	0		ns
t_{RIH}[4]	$\overline{R_0}$·$\overline{R_7}$ Hold Time After $\overline{INT}$	35	20		ns
t_{RA}	$\overline{R_0}$·$\overline{R_7}$ to $\overline{A_0}$·$\overline{A_2}$ Propagation Delay		80	100	ns
t_{ELA}	$\overline{ELR}$ to $\overline{A_0}$·$\overline{A_2}$ Propagation Delay		40	55	ns
t_{ECA}	$\overline{ECS}$ to $\overline{A_0}$·$\overline{A_2}$ Propagation Delay		100	130	ns
t_{ETA}	ETLG to $\overline{A_0}$·$\overline{A_2}$ Propagation Delay		35	70	ns
t_{DECS}[4]	$\overline{SGS}$ and $\overline{B_0}$·$\overline{B_2}$ Setup Time to $\overline{ECS}$	20	10		ns
t_{DECH}[4]	$\overline{SGS}$ and $\overline{B_0}$·$\overline{B_2}$ Hold Time After $\overline{ECS}$	20	10		ns
t_{REN}	$\overline{R_0}$·$\overline{R_7}$ to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	30	ns
t_{ECRN}	$\overline{ECS}$ to ENLG Propagation Delay		85	110	ns
t_{ECSN}	$\overline{ECS}$ to ENLG Propagation Delay		35	55	ns

CAPACITANCE

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max	
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance Except ENLG (Pin 14)		7	12	pF

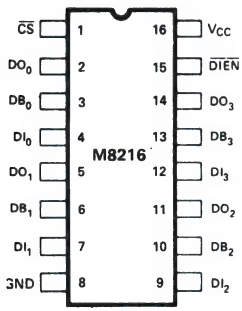
Test Conditions: V_{BIAS} = 2.5V, V_{CC} = 5V, T_A = 25°C, f = 1 MHz

M8216/M8226
4-BIT PARALLEL BIDIRECTIONAL BUS DRIVER

- **Data Bus Buffer Driver for 8080 CPU**
- **Low Input Load Current: 0.25mA Maximum**
- **High Output Drive Capability for Driving System Data Bus**
- **16-Pin Dual In-Line Package**
- **3.40V Output High Voltage for Direct Interface to 8080 CPU**
- **3-State Outputs**
- **Full Military Temperature Range -55°C to +125°C**
- **±10% Power Supply Tolerance**

The M8216/M8226 is a 4-bit bidirectional bus driver/receiver. All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.40V V_{OH}, and for high capacitance terminated bus structures, the DB outputs provide a high 50 mA I_{OL} capability. A non-inverting (M8216) and an inverting (M8226) are available to meet a wide variety of applications for buffering in microcomputer systems.

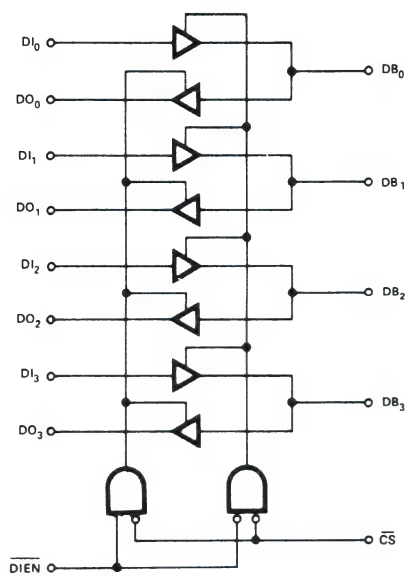
PIN CONFIGURATION



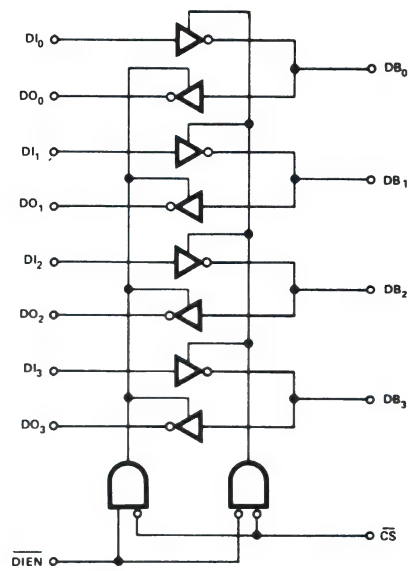
PIN NAMES

DB_0-DB_3	DATA BUS BI-DIRECTIONAL
DI_0-DI_3	DATA INPUT
DO_0-DO_3	DATA OUTPUT
$\overline{DIEN}$	DATA IN ENABLE DIRECTION CONTROL
$\overline{CS}$	CHIP SELECT

LOGIC DIAGRAM
M8216



LOGIC DIAGRAM
M8226



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +160°C
All Output and Supply Voltages . . . . . −0.5V to +7V
All Input Voltages . . . . . −1.0V to +5.5V
Output Currents . . . . . 125 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

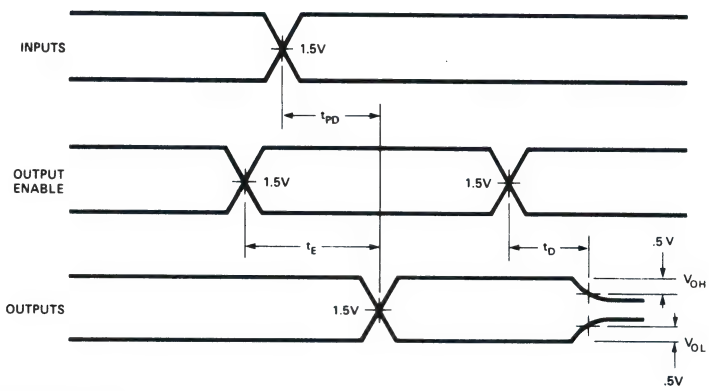
D.C. AND OPERATING CHARACTERISTICS

T_A = -55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Conditions
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		-0.15	-.5	mA	V_F = 0.45
I_{F2}	Input Load Current All Other Inputs		-0.08	-.25	mA	V_F = 0.45
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$			20	μA	V_R = 5.5V
I_{R2}	Input Leakage Current DI Inputs			10	μA	V_R = 5.5V
V_C	Input Forward Voltage Clamp			-1.2	V	I_C = -5mA
V_{IL}	Input "Low" Voltage M8216			.95	V	V_{CC} = 5V
V_{IL}	Input "Low" Voltage M8226			.90	V	V_{CC} = 5V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5V
$\|I_O\|$	Output Leakage Current (3-State) DO DB			20 100	μA	V_O = .45V to V_{CC}
I_{CC}	Power Supply Current M8216		95	130	mA	
I_{CC}	Power Supply Current M8226		85	120	mA	
V_{OL1}	Output "Low" Voltage		0.3	.45	V	DO Outputs I_{OL} = 15mA DB Outputs I_{OL} = 25mA
V_{OL2}	Output "Low" Voltage		0.5	.6	V	DB Outputs I_{OL} = 45mA
V_{OH}	Output "High" Voltage	3.4	3.8		V	DO Outputs I_{OH} = -.5mA
V_{OH2}	Output "High" Voltage	2.4	3.0		V	DO Outputs I_{OH} = -2mA DB Outputs I_{OH} = -5.0mA
I_{OS}	Output Short Circuit Current	-15 -30	-35 -75	-65 -120	mA mA	DO Outputs V_{CC} = 5.0V DB Outputs V_{CC} = 5.0V

NOTE: Typical values are for T_A = 25°C, V_{CC} = 5.0V.

WAVEFORMS



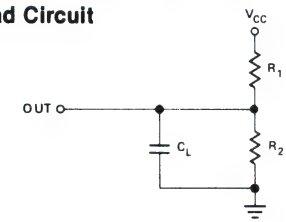
A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = +5V ±10%

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
T_{PD1}	Input to Output Delay DO Outputs		15	25	ns	(NOTE 2)
T_{PD2}	Input to Output Delay DB Outputs M8216		19	33	ns	(NOTE 2)
T_{PD2}	Input to Output Delay DB Outputs M8226		16	25	ns	(NOTE 2)
T_E	Output Enable Time M8216		42	75	ns	(NOTE 2)
T_E	Output Enable Time M8226		36	62	ns	(NOTE 2)
T_D	Output Disable Time M8216		16	40	ns	(NOTE 2)
T_D	Output Disable Time M8226		16	38	ns	(NOTE 2)

Test Conditions

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.

Test Load Circuit



CAPACITANCE

Symbol	Parameter		Limits			Unit
			Min.	Typ.[1]	Max.	
C_{IN}	Input Capacitance			4	6	pF
C_{OUT1}	Output Capacitance	DO Outputs		6	10	pF
C_{OUT2}	Output Capacitance	DB Outputs		13	18	pF

Test Conditions: V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz.

NOTES: 1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.

2.

TEST	C_L	R_1	R_2
T_{PD1}	30pF	300Ω	600Ω
T_{PD2}	300pF	90Ω	180Ω
T_E, (DO, ENABLE↑)	30pF	10KΩ	1KΩ
T_E, (DO, ENABLE↓)	30pF	300Ω	600Ω
T_E, (DB, ENABLE↑)	300pF	10KΩ	1KΩ
T_E, (DB, ENABLE↓)	300pF	90Ω	180Ω
T_D, (DO, DISABLE↑)	5pF	300Ω	600Ω
T_D, (DO, DISABLE↓)	5pF	10KΩ	1KΩ
T_D, (DB, DISABLE↑)	5pF	90Ω	180Ω
T_D, (DB, DISABLE↓)	5pF	10KΩ	1KΩ

M8224
CLOCK GENERATOR AND DRIVER FOR 8080A CPU

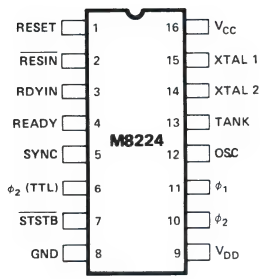
- **Single Chip Clock Generator/Driver for M8080A CPU**
- **Power-Up Reset for CPU**
- **Ready Synchronizing Flip-Flop**
- **Advanced Status Strobe**
- **Fully Military Temperature Range −55°C to +125°C**
- **Oscillator Output for External System Timing**
- **Crystal Controlled for Stable System Operation**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**

The Intel® M8224 is a single chip clock generator/driver for the M8080A CPU. It is controlled by a crystal, selected by the designer to meet a variety of system speed requirements.

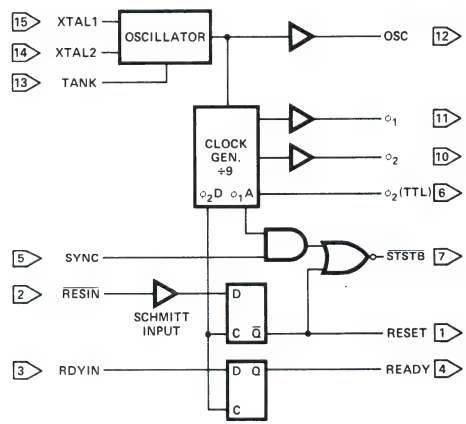
Also included are circuits to provide power-up reset, advance status trobe, and synchronization of ready.

The M8224 provides the designer with a significant reduction of packages used to generate clocks and timing for M8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

RESIN	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
STSTB	STATUS STB (ACTIVE LOW)
φ1	8080 CLOCKS
φ2	8080 CLOCKS

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	CONNECTIONS FOR CRYSTAL
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
φ2 (TTL)	φ2 CLK (TTL LEVEL)
VCC	+5V
VDD	+12V
GND	0V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -55°C to 125°C
Storage Temperature . . . . . -65°C to 150°C
Supply Voltage, V_{CC} . . . . . -0.5V to +7V
Supply Voltage, V_{DD} . . . . . -0.5V to +13.5V
Input Voltage . . . . . -1.0V to +7V
Output Current 100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = −55°C to 125°C; V_{CC} = +5.0V ±10%; V_{DD} = +12V ±10%.

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
I_F	Input Current Loading			-.25	mA	V_F = .45V
I_R	Input Leakage Current			10	μA	V_R = 5.5V
V_C	Input Forward Clamp Voltage			−1.2	V	I_C = -5mA
V_{IL}	Input "Low" Voltage			.8	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage $\overline{RESIN}$ All Other Inputs	2.6 2.0			V	
V_{IH}-V_{IL}	$\overline{RESIN}$ Input Hysteresis	.25			V	V_{CC} = 5.0V
V_{OL}	Output "Low" Voltage OSC, ϕ2 (TTL) All Other Outputs			.45 .45	V V	I_{OL} = 10mA I_{OL} = 2.5mA
V_{OH}	Output "High" Voltage ϕ_1 , ϕ_2 READY, RESET OSC, ϕ2 (TTL), $\overline{STSTB}$	 9.0 3.3 2.4			 V V V	 I_{OH} = -100μA I_{OH} = -100μA I_{OH} = -1mA
I_{OS}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	-10		-60	mA	V_O = 0V V_{CC} = 5.0V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Note: 1. Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

Crystal Requirements

Tolerance: .005% at -55°C to 125°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4mW

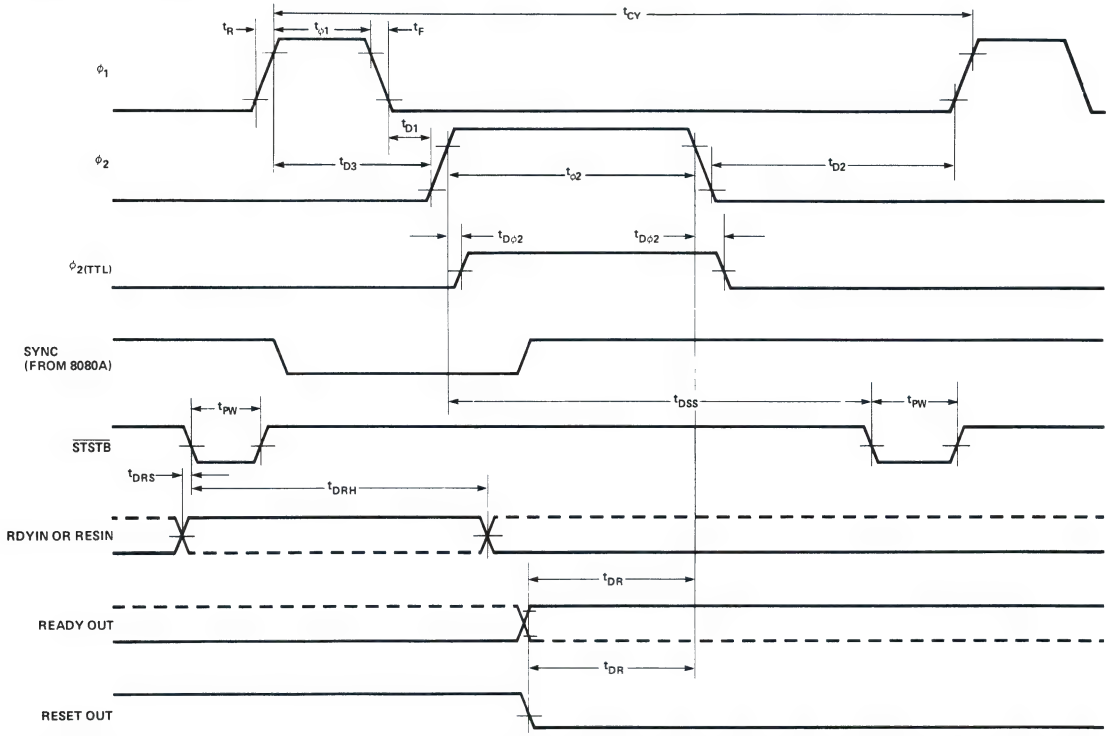
*With tank circuit use 3rd overtone mode.

A.C. CHARACTERISTICS

V_{CC} = +5.0 ±10%; V_{DD} = +12.0V ±10%; T_A = −55°C to +125°C

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
$t_{\phi 1}$	ϕ_1 Pulse Width	$\frac{2tcy}{9}$ − 20ns			ns	C_L = 20pF to 50pF
$t_{\phi 2}$	ϕ_2 Pulse Width	$\frac{5tcy}{9}$ − 45ns				
t_{D1}	ϕ_1 to ϕ_2 Delay	0				
t_{D2}	ϕ_2 to ϕ_1 Delay	$\frac{2tcy}{9}$ − 25ns				
t_{D3}	ϕ_1 to ϕ_2 Delay	$\frac{2tcy}{9}$		$\frac{2tcy}{9}$ + 40ns		
t_R	ϕ_1 and ϕ_2 Rise Time			25		
t_F	ϕ_1 and ϕ_2 Fall Time			25		
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	ϕ_2TTL,CL=30pF R_1=300Ω R_2=600Ω
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\frac{6tcy}{9}$ − 30ns		$\frac{6tcy}{9}$		$\overline{STSTB}$, CL=15pF R_1 = 2K R_2 = 4K
t_{PW}	$\overline{STSTB}$ Pulse Width	$\frac{tcy}{9}$ − 23ns				
t_{DRS}	RDYIN Setup Time to Status Strobe	50ns − $\frac{4tcy}{9}$				
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$	$\frac{4tcy}{9}$				
t_{DR}	READY or RESET to ϕ_2 Delay	$\frac{4tcy}{9}$ − 25ns				CL=10pF R_1=2K R_2=4K
t_{CLK}	CLK Period		$\frac{tcy}{9}$			
f_{max}	Maximum Oscillating Frequency	27			MHz	
C_{in}	Input Capacitance			8	pF	V_{CC}=+5.0V V_{DD}=+12V V_{BIAS}=2.5V f=1MHz

WAVEFORMS



VOLTAGE MEASUREMENT POINTS: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 7.0V. READY, RESET Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

Example:

A.C. CHARACTERISTICS (For t_{CY} = 488.28 ns.)

T_A = −55°C to 125°C; V_{CC} = +5.0V ±10%; V_{DD} = +12V ± 10%

Symbol	Parameter	Limits Min.	Typ.	Max.	Units	Test Conditions
$t_{\phi 1}$	ϕ_1 Pulse Width	89			ns	t_{CY}=488.28ns
$t_{\phi 2}$	ϕ_2 Pulse Width	226			ns	
t_{D1}	Delay ϕ_1 to ϕ_2	0			ns	
t_{D2}	Delay ϕ_2 to ϕ_1	84			ns	ϕ_1 & ϕ_2 Loaded to C_L = 20 to 50pF
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges	109		149	ns	
t_r	Output Rise Time			25	ns	
t_f	Output Fall Time			25	ns	
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	296		326	ns	
$t_{D\phi 2}$	ϕ_2 to ϕ_2 (TTL) Delay	-5		+15	ns	
t_{PW}	Status Strobe Pulse Width	31			ns	Ready & Reset Loaded to 2mA/10pF
t_{DRS}	RDYIN Setup Time to $\overline{STSTB}$	-167			ns	All measurements referenced to 1.5V unless specified otherwise.
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$	217			ns	
t_{DR}	READY or RESET to ϕ_2 Delay	192			ns	

M8228
SYSTEM CONTROLLER AND BUS DRIVER FOR M8080A CPU

- **Single Chip System Control for MCS-80™ Systems**
- **Built-In Bidirectional Bus Driver for Data Bus Isolation**
- **Allows the Use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **User Selected Single Level Interrupt Vector (RST 7)**
- **28-Pin Dual In-Line Package**
- **Reduces System Package Count**
- **Full Military Temperature Range −55°C to +125°C**
- **±10% Power Supply Tolerance**

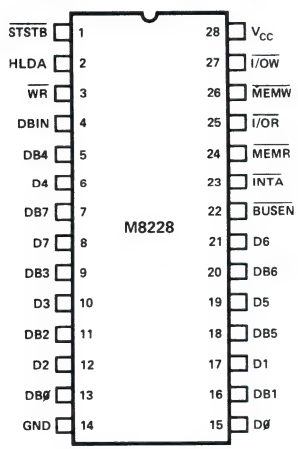
The Intel® M8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bidirectional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

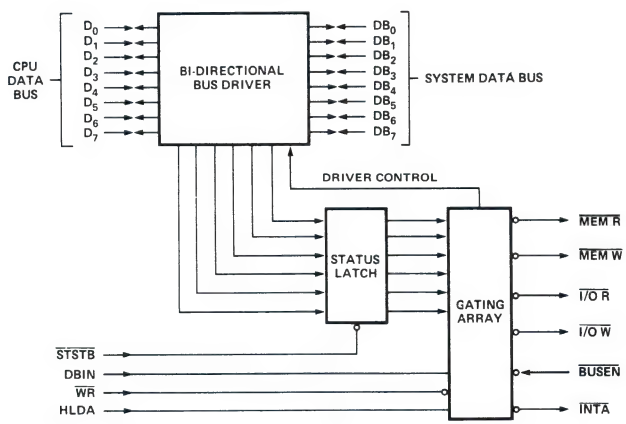
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The M8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an interrupt acknowledge by the M8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The M8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	$\overline{INTA}$	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
$\overline{I/OR}$	I/O READ	$\overline{WR}$	WR (FROM 8080)
$\overline{I/OW}$	I/O WRITE	$\overline{BUSEN}$	BUS ENABLE INPUT
$\overline{MEMR}$	MEMORY READ	$\overline{STSTB}$	STATUS STROBE (FROM 8224)
$\overline{MEMW}$	MEMORY WRITE	V_{CC}	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -55°C to 125°C
Storage Temperature . . . . . -65°C to 150°C
Supply Voltage, V_{CC} . . . . . -0.5V to +7V
Input Voltage . . . . . -1.0V to +7V
Output Current 100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = -55°C to 125°C; V_{CC} = 5V ±10%.

Symbol	Parameter	Limits Min.	Limits Max.	Unit	Test Conditions
V_C	Input Clamp Voltage, All Inputs		-1.2	V	I_C = -5mA
I_F	Input Load Current, $\overline{STSTB}$		500	μA	V_F = 0.4V
	D_2, D_6		750	μA	
	D_0, D_1, D_4, D_5, D_7		250	μA	
	All Other Inputs		250	μA	
I_R	Input Leakage Current $DB_0 - D_7$		20	μA	V_R = 5.5V
	All Other Inputs		100	μA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8	2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		210	mA	
V_{OL}	Output Low Voltage, $D_0 - D_7$		.5	V	I_{OL} = 2mA
	All Other Outputs		.5	V	I_{OL} = 10mA
V_{OH}	Output High Voltage, $D_0 - D_7$	3.3		V	I_{OH} = -10μA
	All Other Outputs	2.4		V	I_{OH} = -1mA
I_{OS}	Short Circuit Current, All Outputs	15	90	mA	V_{CC} = 5V
$I_{O\ (Off)}$	Off State Output Current, All Controls Outputs		100	μA	V_O = 5.5V
			-100	μA	V_O = .45V
I_{INT}	$\overline{INTA}$ Current		5	mA	(See Figure 1)

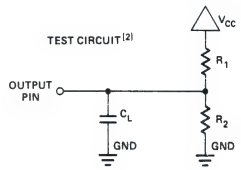
Note 1: Typical values are for T_A = 25°C and nominal supply voltages.

CAPACITANCE This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25°C$, f = 1MHz.

Note 2: For D_0-D_7: $R_1 = 4K\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$. For all other outputs: $R_1 = 500\Omega$, $R_2 = 1K\Omega$, $C_L = 100pF$.



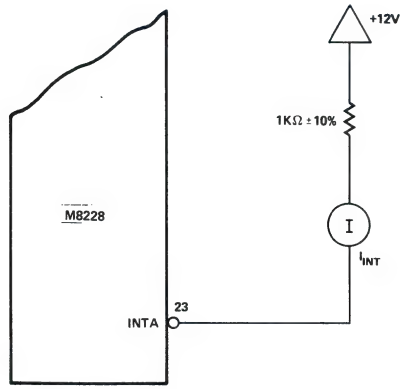


Figure 1. INTA Test Circuit (for RST 7)

A.C. CHARACTERISTICS $T_A = -55°C$ to $125°C$; $V_{CC} = 5V \pm 10\%$.

Symbol	Parameter	Limits Min.	Max.	Units	Condition
t_{PW}	Width of Status Strobe	25		ns	
t_{SS}	Setup Time, Status Inputs D_0-D_7	8		ns	
t_{SH}	Hold Time, Status Inputs D_0-D_7	5		ns	
t_{DC}	Delay from $\overline{STSTB}$ to any Control Signal	20	75	ns	$C_L = 100pF$
t_{RR}	Delay from DBIN to Control Outputs		30	ns	$C_L = 100pF$
t_{RE}	Delay from DBIN to Enable/Disable 8080 Bus		45	ns	$C_L = 25pF$
t_{RD}	Delay from System Bus to 8080 Bus during Read		45	ns	$C_L = 25pF$
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	5	60	ns	$C_L = 100pF$
t_{WE}	Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$		30	ns	$C_L = 100pF$
t_{WD}	Delay from 8080 Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	5	40	ns	$C_L = 100pF$
t_E	Delay from System Bus Enable to System Bus DB_0-DB_7		30	ns	$C_L = 100pF$
t_{HD}	HLDA to Read Status Outputs		25	ns	$C_L = 100pF$
t_{DS}	Setup Time, System Bus Inputs to HLDA	10		ns	
t_{DH}	Hold Time, System Bus Inputs to HLDA	20		ns	

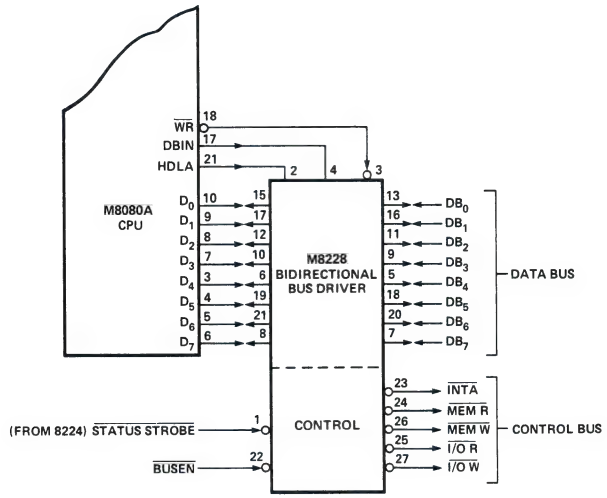


Figure 2. M8080A CPU Interface

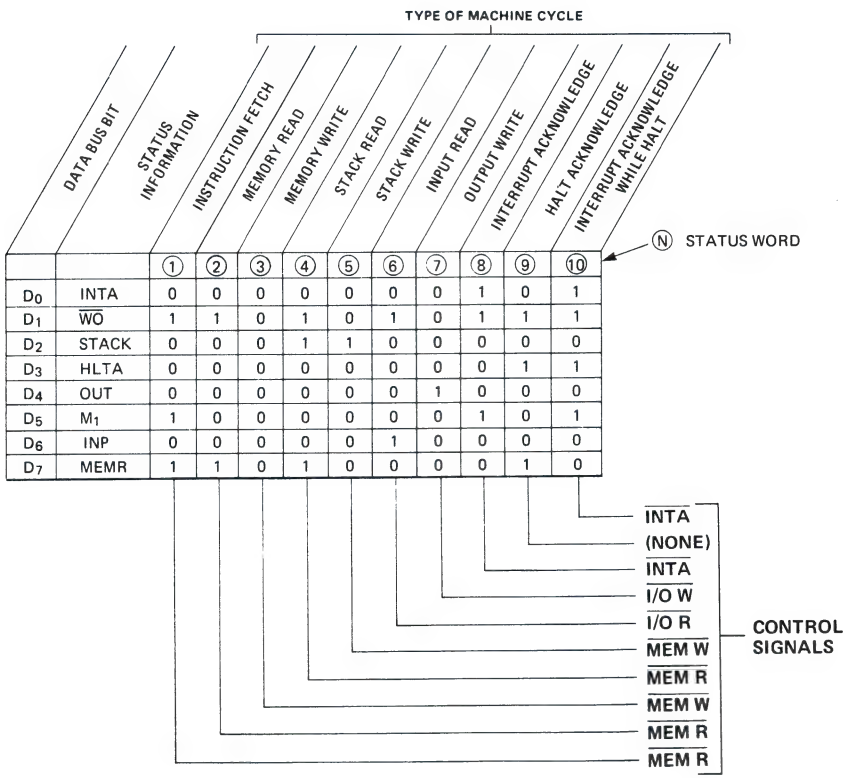
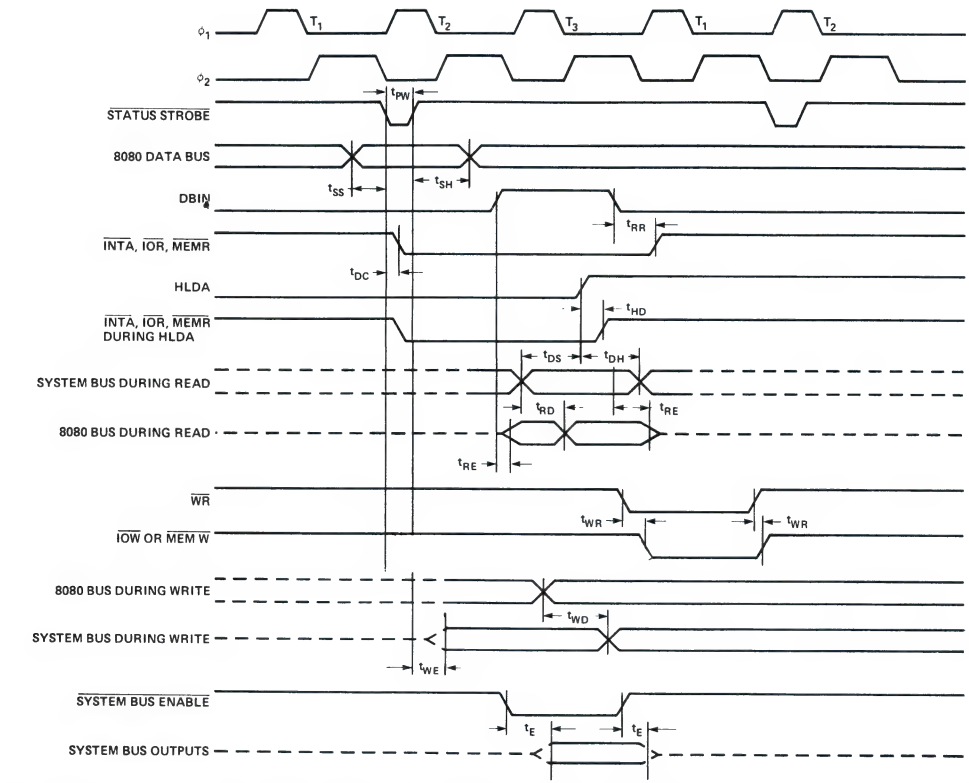


Figure 3. Status Word Chart

WAVEFORMS



VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

M8085A
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

- **Single +5V Power Supply**
- **100% Software Compatible with 8080A**
- **1.3 μs Instruction Cycle**
- **On-Chip Clock Generator (with External Crystal, LC or RC Network)**
- **On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control**
- **Four Vectored Interrupt Inputs (One is non-Maskable) Plus an 8080A-compatible interrupt**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capability to 64k Bytes of Memory**

The Intel® M8085A is a complete 8-bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed.

The M8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The M8085A uses a multiplexed data bus. The address is split between the 8-bit address bus and the 8-bit data bus.

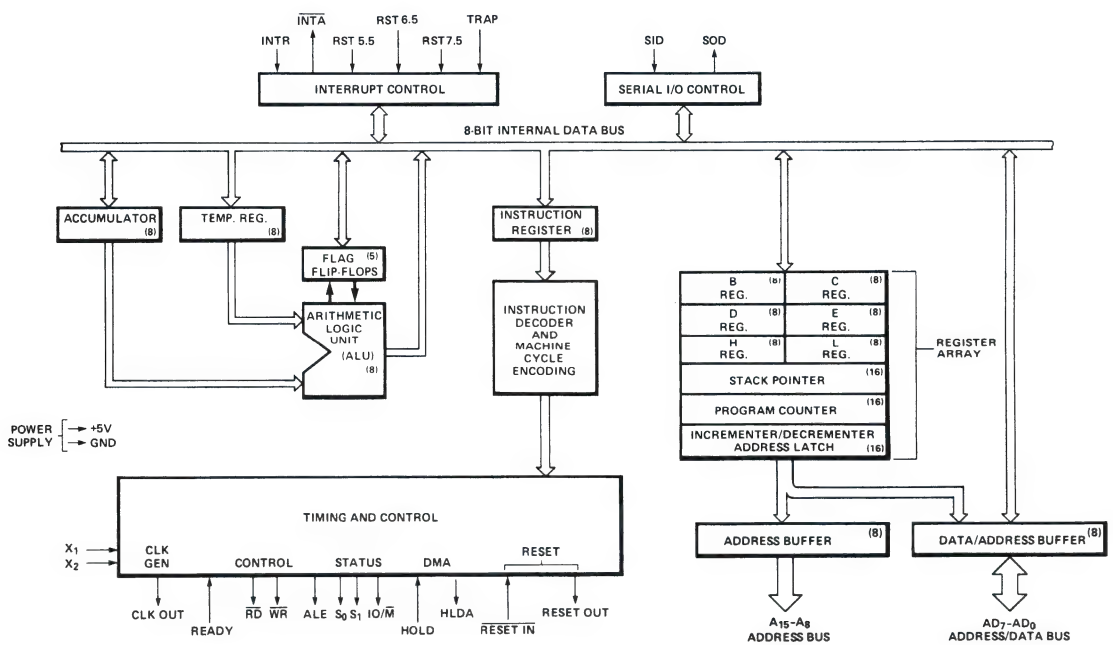


Figure 1. M8085A CPU Functional Block Diagram.

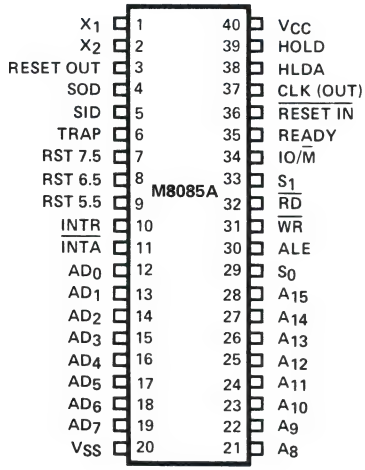


Figure 2. M8085A Pinout Diagram

M8085A FUNCTIONAL PIN DESCRIPTION

The following describes the function of each pin:

Symbol	Function
A_8–A_{15} (Output, 3-state)	Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_{0-7} (Input/Output, 3-state)	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE (Output)	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1, and IO/$\overline{M}$ (Output)	Machine cycle status:

IO/$\overline{M}$	S_1	S_0	Status
0	0	1	Memory write
0	1	0	Memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch
1	1	1	Interrupt Acknowledge
*	0	0	Halt
*	X	X	Hold
*	X	X	Reset

* = 3-state (high impedance)
X = unspecified

Symbol	Function
	S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$,S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$ (Output, 3-state)	READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$ (Output, 3-state)	WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.
READY (Input)	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle.
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA (Output)	HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR (Input)	INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

M8085A FUNCTIONAL PIN DESCRIPTION (Continued)

Symbol	Function
$\overline{\text{INTA}}$ (Output)	INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) $\overline{\text{RD}}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.
RST 5.5 **RST 6.5** **RST 7.5** **(Inputs)**	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP (Input)	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 1.)
$\overline{\text{RESET IN}}$ (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT (Output)	Indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

TABLE 1. INTERRUPT PRIORITY, RESTART ADDRESS, AND SENSITIVITY

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

NOTES:

(1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

FUNCTIONAL DESCRIPTION

The M8085A is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz, thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The CPU (8085A), a RAM/IO (8156), and a ROM or EPROM/IO chip (8355 or 8755A).

The M8085A has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The M8085A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC,DE,HL	General-Purpose Registers; data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The M8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The M8085A provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD, READY, and all Interrupts are synchronized with the processor's internal clock. The M8085A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the M8085A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

INTERRUPT AND SERIAL I/O

The M8085A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 1.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are *high level-sensitive* like INTR (and INT on the 8080) and are recognized with the same timing as INTR. RST 7.5 is *rising edge-sensitive.*

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. (See Section 2.2.7.) The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the M8085A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and $\overline{RESET\ IN}$. (See SIM, Chapter 4.)

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP — highest priority, RST 7.5, RST 6.5, RST 5.5, INTR — lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both *edge and level sensitive.* The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 3 illustrates the TRAP interrupt request circuitry within the M8085A. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

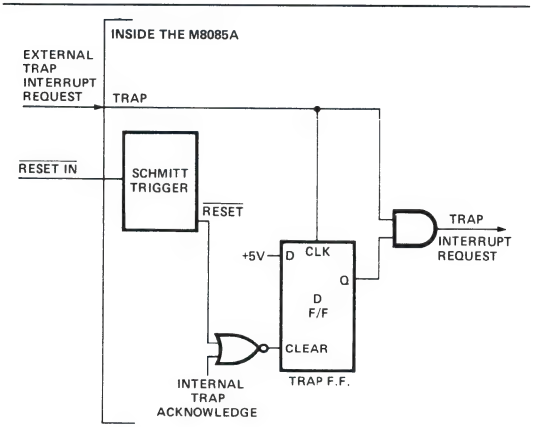


Figure 3. TRAP and $\overline{RESET\ IN}$ Circuit

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST 5.5–7.5 will provide current Interrupt Enable status, revealing that Interrupts are disabled. See the description of the RIM instruction in Chapter 4.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

BASIC SYSTEM TIMING

The M8085A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 4 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 2.) The status lines can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless WAIT or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.

TABLE 2. M8085A MACHINE CYCLE CHART

MACHINE CYCLE		STATUS			CONTROL		
		$IO/\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH	(OF)	0	1	1	0	1	1
MEMORY READ	(MR)	0	1	0	0	1	1
MEMORY WRITE	(MW)	0	0	1	1	0	1
I/O READ	(IOR)	1	1	0	0	1	1
I/O WRITE	(IOW)	1	0	1	1	0	1
ACKNOWLEDGE OF INTR	(INA)	1	1	1	1	1	0
BUS IDLE	(BI): DAD	0	1	0	1	1	1
	ACK. OF RST,TRAP	1	1	1	1	1	1
	HALT	TS	0	0	TS	TS	1

TABLE 3. M8085A MACHINE STATE CHART

Machine State	Status & Buses				Control		
	S1,S0	$IO/\overline{M}$	A_8-A_{15}	AD_0-AD_7	$\overline{RD}$,$\overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1*
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0†	X	TS	1	1	0
T_5	1	0†	X	TS	1	1	0
T_6	1	0†	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0"
1 = Logic "1"
TS = High Impedance
X = Unspecified

* ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
† IO/M = 1 during T_4-T_6 of INA machine cycle.

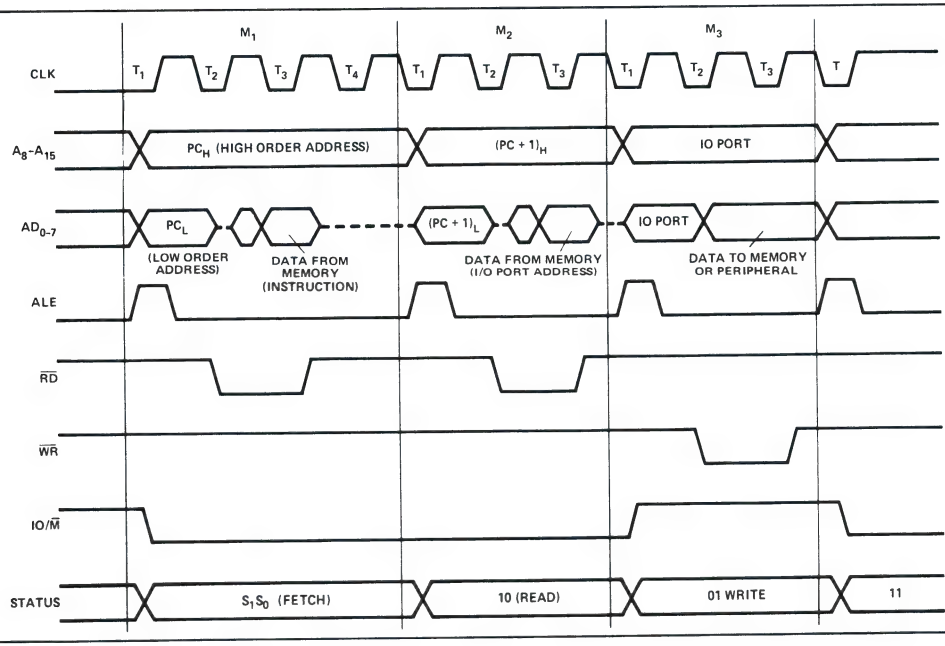


Figure 4. M8085A Basic System Timing

TABLE 4. ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . .–55°C to +125°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1.5 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 4. D.C. CHARACTERISTICS

(T_A = -55°C to +125°C; V_{CC} = 5V ±10%; V_{SS} = 0V; unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	+0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{CC}	Power Supply Current		200	mA	
I_{IL}	Input Leakage		±10	μA	$V_{in} = V_{CC}$
I_{LO}	Output Leakage		±10	μA	$0.45V \leqslant V_{out} \leqslant V_{CC}$
V_{ILR}	Input Low Level, RESET	-0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC} +0.5	V	
V_{HY}	Hysteresis, RESET	0.25		V	

TABLE 5. A.C. CHARACTERISTICS

T_A = -55°C to +125°C, V_{CC} = 5V ±10%; V_{SS} = 0V

Symbol	Parameter	M8085A[2]		Units
		Min.	Max.	
t_{CYC}	CLK Cycle Period	320	2000	ns
t_1	CLK Low Time	80		ns
t_2	CLK High Time	120		ns
t_r,t_f	CLK Rise and Fall Time		30	ns
t_{XKR}	X_1 Rising to CLK Rising	30	120	ns
t_{XKF}	X_1 Rising to CLK Falling	30	150	ns
t_{AC}	A_{8-15} Valid to Leading Edge of Control[1]	270		ns
t_{ACL}	A_{0-7} Valid to Leading Edge of Control	240		ns
t_{AD}	A_{0-15} Valid to Valid Data In		575	ns
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0	ns
t_{AL}	A_{8-15} Valid Before Trailing Edge of ALE[1]	90		ns
t_{ALL}	A_{0-7} Valid Before Trailing Edge of ALE	70		ns
t_{ARY}	READY Valid from Address Valid		220	ns
t_{CA}	Address (A_8-A_{15}) Valid After Control	120		ns
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) Edge of ALE	400		ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		ns
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		ns
t_{HABE}	HLDA to Bus Enable		210	ns
t_{HABF}	Bus Float After HLDA		210	ns
t_{HACK}	HLDA Valid to TRailing Edge of CLK	110		ns
t_{HDH}	HOLD Hold Time	0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		ns
t_{INH}	INTR Hold Time	0		ns
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		ns
t_{LA}	Address Hold Time After ALE	100		ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		ns
t_{LCK}	ALE Low During CLK High	100		ns
t_{LDR}	ALE to Valid Data During Read		460	ns
t_{LDW}	ALE to Valid Data During Write		200	ns
t_{LL}	ALE Width	140		ns
t_{LRY}	ALE to READY Stable		110	ns

TABLE 5. A.C. CHARACTERISTICS (Cont.)

Symbol	Parameter	M8085A[2]		Units
		Min.	Max.	
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150		ns
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		300	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		ns
t_{RDH}	Data Hold Time After $\overline{READ}$ $\overline{INTA}$ [7]	0		ns
t_{RYH}	READY Hold Time	0		ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	100		ns
t_{WDL}	LEADING Edge of WRITE to Data Valid		40	ns

Notes:
1. A_8-A_{15} address Specs apply to IO/$\overline{M}$, S_0, and S_1 except A_8-A_{15} are undefined during T_4-T_6 of OF cycle whereas IO/$\overline{M}$, S_0, and S_1 are stable.
2. Test conditions: t_{CYC} = 320ns; C_L = 150pF.
3. For all output timing where C_L = 150pF use the following correction factors:
   25pF ≤ C_L < 150pF: -0.10 ns/pF
   150pF < C_L ≤ 300pF: +0.30 ns/pF
4. Output timings are measured with purely capacitive load.
5. All timings are measured at output voltage V_L = 0.8V, V_H = 2.0V, and 1.5V with 20ns rise and fall time on inputs.
6. To calculate timing specifications at other values of t_{CYC} use Table 6.
7. Data hold time is guaranteed under all loading conditions.

TABLE 6. BUS TIMING SPECIFICATION AS A T_{CYC} DEPENDENT

M8085A

t_{AL}	–	(1/2) T - 45	MIN
t_{LA}	–	(1/2) T - 60	MIN
t_{LL}	–	(1/2) T - 20	MIN
t_{LCK}	–	(1/2) T - 60	MIN
t_{LC}	–	(1/2) T - 30	MIN
t_{AD}	–	(5/2 + N) T - 225	MAX
t_{RD}	–	(3/2 + N) T - 180	MAX
t_{RAE}	–	(1/2) T - 10	MIN
t_{CA}	–	(1/2) T - 40	MIN
t_{DW}	–	(3/2 + N) T – 60	MIN
t_{WD}	–	(1/2) T - 60	MIN
t_{CC}	–	(3/2 + N) T - 80	MIN
t_{CL}	–	(1/2) T - 110	MIN
t_{ARY}	–	(3/2) T - 260	MAX
t_{HACK}	–	(1/2) T - 50	MIN
t_{HABF}	–	(1/2) T + 50	MAX
t_{HABE}	–	(1/2) T + 50	MAX
t_{AC}	–	(2/2) T - 50	MIN
t_1	–	(1/2) T - 80	MIN
t_2	–	(1/2) T - 40	MIN
t_{RV}	–	(3/2) T - 80	MIN
t_{LDR}	–	(4/2) T - 180	MAX

NOTE: N is equal to the total WAIT states.
$T = t_{CYC}$.

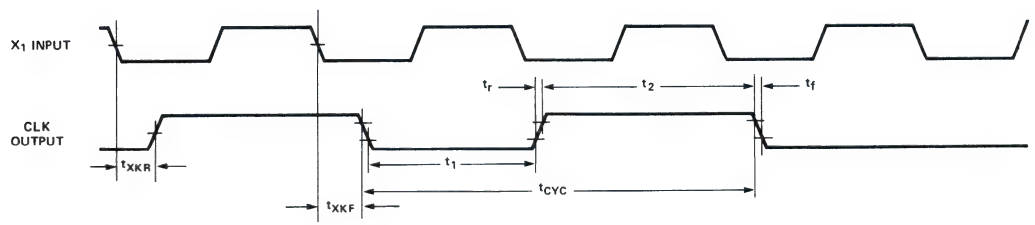
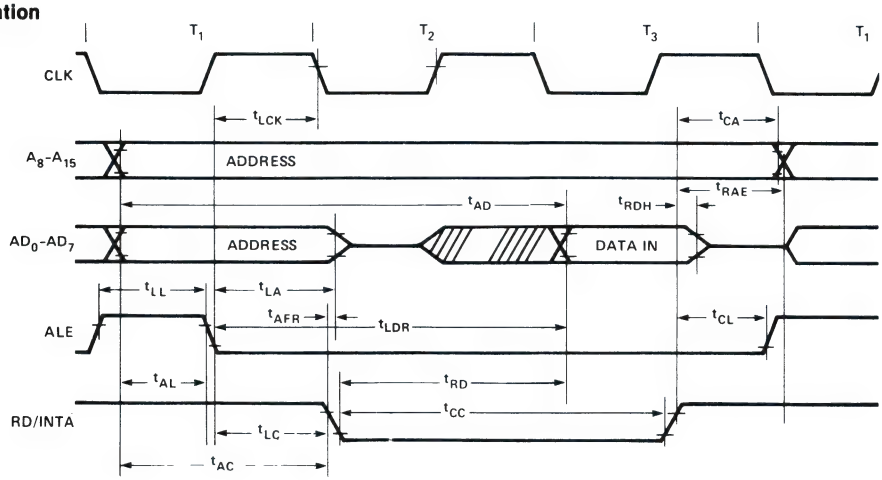
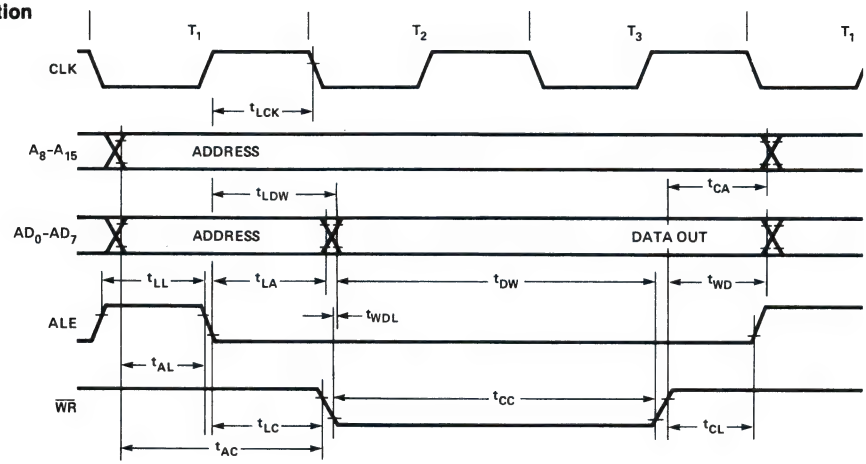


Figure 5. Clock Timing Waveform

Read Operation



Write Operation



Read operation with Wait Cycle (Typical) — same READY timing applies to WRITE operation.

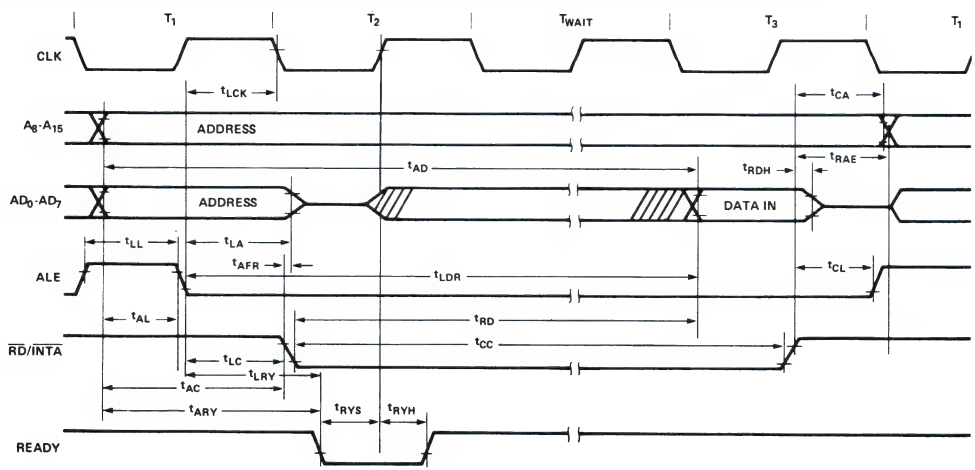


Figure 6. M8085A Bus Timing, With and Without Wait

Hold Operation

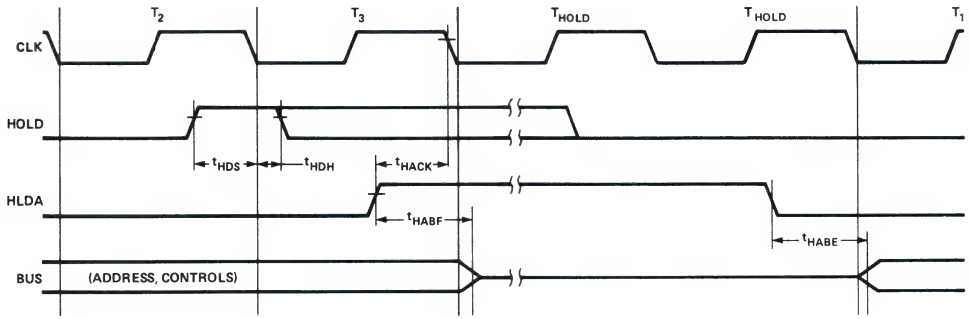


Figure 7. M8085A Hold Timing

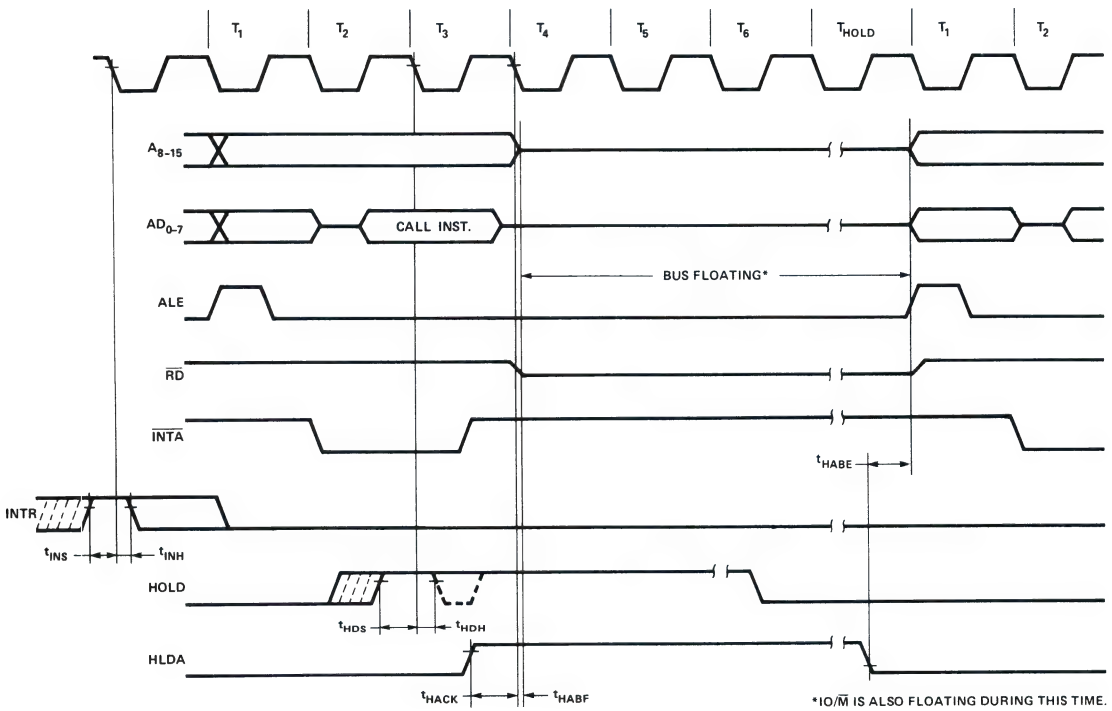


Figure 8. M8085A Interrupt and Hold Timing

M8155
2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

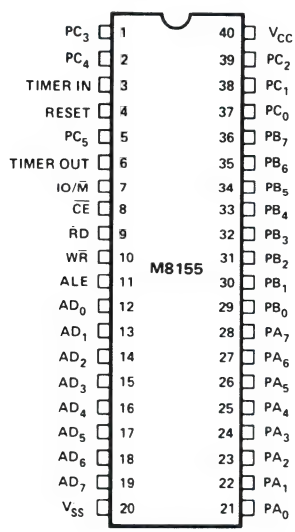
- **Military Temperature Range Operation (-55° C TO +125° C)**
- **256 Word x 8 Bits**
- **Single +5V Power Supply**
- **Completely Static Operation**
- **Internal Address Latch**
- **2 Programmable 8 Bit I/O Ports**
- **1 Programmable 6-Bit I/O Port**
- **Programmable 14-Bit Binary Counter/ Timer**
- **Multiplexed Address and Data Bus**
- **40 Pin DIP**

The M8155 is a RAM and I/O chip to be used in the MCS-85™ microcomputer system. The RAM portion is designed with 2048 static cells organized as 256 x 8. It has a maximum access time of 400 ns to permit use with no wait states in the 8085A CPU.

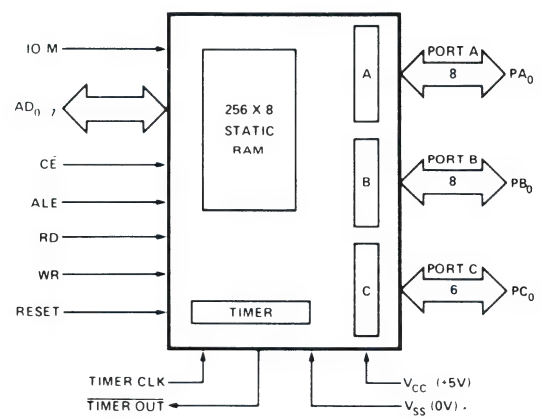
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

PIN CONFIGURATION



BLOCK DIAGRAM



M8155 PIN FUNCTIONS

Symbol	Function
RESET (input)	Pulse provided by the 8085A to initialize the system (connect to 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085A clock cycle times.
AD_{0-7} (input)	3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the M8155 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
$\overline{CE}$ (input)	Chip Enable: On the M8155, this pin is $\overline{CE}$ and is ACTIVE LOW.
$\overline{RD}$ (input)	Read control: Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$ (input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on IO/$\overline{M}$.
ALE (input)	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$ (input)	Selects memory if low and I/O and command/status registers if high.
PA_{0-7}(8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB_{0-7}(8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC_{0-5}(6) (input/output)	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 — A INTR (Port A Interrupt) PC_1 — $\overline{ABF}$ (Port A Buffer Full) PC_2 — $\overline{A\ STB}$ (Port A Strobe) PC_3 — B INTR (Port B Interrupt) PC_4 — $\overline{B\ BF}$ (Port B Buffer Full) PC_5 — B STB (Port B Strobe)
TIMER IN (input)	Input to the counter-timer.
$\overline{TIMER\ OUT}$ (output)	Timer output. This output can be either a square wave or a pulse depending on the timer mode.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

DESCRIPTION

The M8155 contains the following:

- 2k Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA & PB) and one 6-bit I/O port (PC)
- 14-bit timer-counter

The IO/$\overline{M}$ (IO/Memory Select) pin selects either the five registers (Command, Status, PA_{0-7}, PB_{0-7}, PC_{0-5}) or the memory (RAM) portion. (See Figure 1.)

The 8-bit address on the Address/Data lines, Chip Enable input CE or $\overline{CE}$, and IO/$\overline{M}$ are all latched on-chip at the falling edge of ALE.

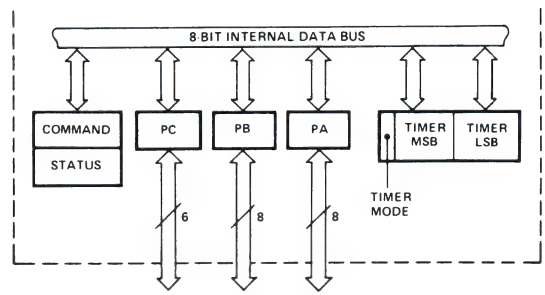


Figure 1. M8155 Internal Registers

PROGRAMMING OF THE COMMAND REGISTER

The command register consists of eight latches. Four bits (0-3) define the mode of the ports, two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The command register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation with the Chip Enable active and IO/$\overline{M}$ = 1. The meaning of each bit of the command byte is defined in Figure 2. The contents of the command register may never be read.

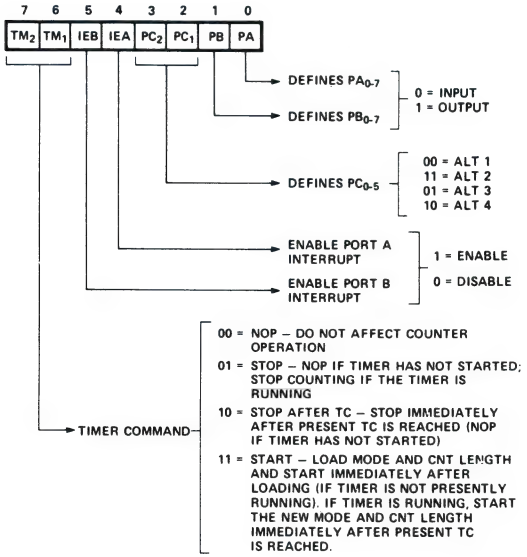


Figure 2. Command Register Bit Assignment

READING THE STATUS REGISTER

The status register consists of seven latches, one for each bit; six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the Status Register (Address XXXXX000). Status word format is shown in Figure 3. Note that you may never write to the status register since the command register shares the same I/O address and the command register is selected when a write to that address is issued.

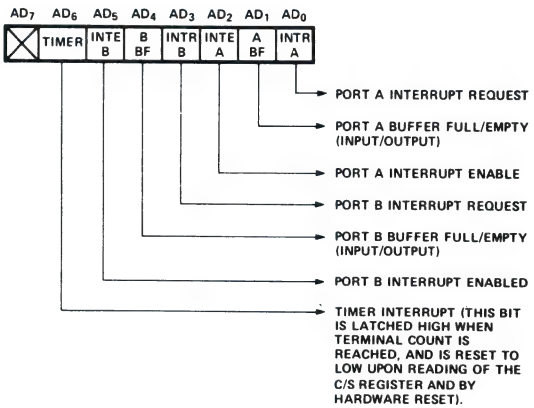


Figure 3. Status Register Bit Assignment

INPUT/OUTPUT SECTION

The I/O section of the M8155 consists of five registers: (See Figure 4.)

- **Command/Status Register (C/S)** — Both registers are assigned the address XXXXX000. The C/S address serves the dual purpose.

  When the C/S registers are selected during WRITE operation, a command is written into the command register. The contents of this register are *not* accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer becomes available on the AD_{0-7} lines.

- **PA Register** — This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (See timing diagram). The I/O pins assigned in relation to this register are PA_{0-7}. The address of this register is XXXXX001.

- **PB Register** — This register functions the same as PA Register. The I/O pins assigned are PB_{0-7}. The address of this register is XXXXX010.

- **PC Register** — This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the AD_2 and AD_3 bits of the C/S register.

  When PC_{0-5} is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the M8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. (See Table 1.)

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

CONTROL	INPUT MODE	OUTPUT MODE
BF	Low	Low
INTR	Low	High
STB	Input Control	Input Control

I/O ADDRESS†								SELECTION
A7	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	0	0	0	Interval Command/Status Register
X	X	X	X	X	0	0	1	General Purpose I O Port A
X	X	X	X	X	0	1	0	General Purpose I O Port B
X	X	X	X	X	0	1	1	Port C — General Purpose I O or Control
X	X	X	X	X	1	0	0	Low-Order 8 bits of Timer Count
X	X	X	X	X	1	0	1	High 6 bits of Timer Count and 2 bits of Timer Mode

X: Don't Care.

†: I/O Address must be qualified by $\overline{CE}$ = 0 (M8155) and IO/$\overline{M}$ = 1 in order to select the appropriate register.

Figure 4. I/O Port and Timer Addressing Scheme

Figure 5 shows how I/O PORTS A and B are structured within the M8155:

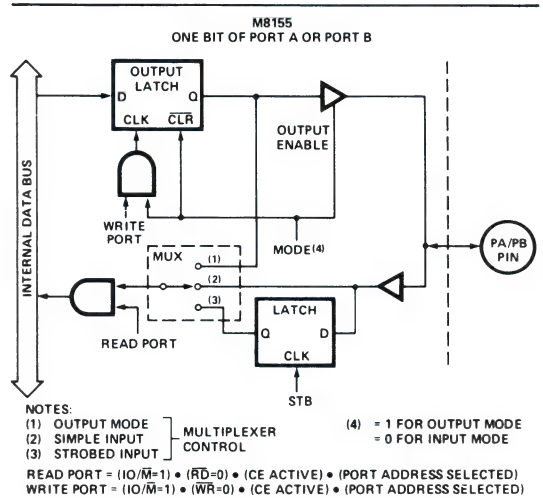


Figure 5. M8155 Port Functions

TABLE 1. TABLE OF PORT CONTROL ASSIGNMENT.

Pin	ALT 1	ALT 2	ALT 3	ALT 4
PC0	Input Port	Output Port	A INTR (Port A Interrupt)	A INTR (Port A Interrupt)
PC1	Input Port	Output Port	A BF (Port A Buffer Full)	A BF (Port A Buffer Full)
PC2	Input Port	Output Port	A $\overline{STB}$ (Port A Strobe)	A $\overline{STB}$ (Port A Strobe)
PC3	Input Port	Output Port	Output Port	B INTR (Port B Interrupt)
PC4	Input Port	Output Port	Output Port	B BF (Port B Buffer Full)
PC5	Input Port	Output Port	Output Port	B $\overline{STB}$ (Port B Strobe)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

The outputs of the M8155 are "glitch-free" meaning that you can write a "1" to a bit position that was previously "1" and the level at the output pin will not change.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to output, the output pins will go low. When the M8155 is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of PORT C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

Figure 6 shows how the M8155 I/O ports might be configured in a typical MCS-85 system.

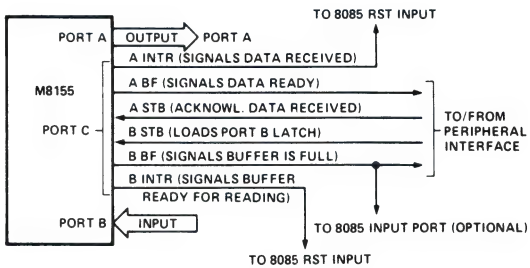


Figure 6. Example: Command Register = 00111001

TIMER SECTION

The timer is a 14-bit down-counter that counts the TIMER IN pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register. (See Figure 4).

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 of the high order count register will specify the length of the next count and bits 14-15 of the high order register will specify the timer output mode (see Figure 7). The value loaded into the count length register can have any value from 2H through 3FFH in Bits 0-13.

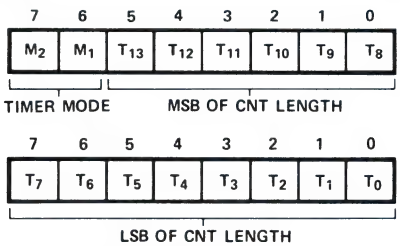


Figure 7. Timer Format

There are four modes to choose from: M2 and M1 define the timer mode, as shown in Figure 9.

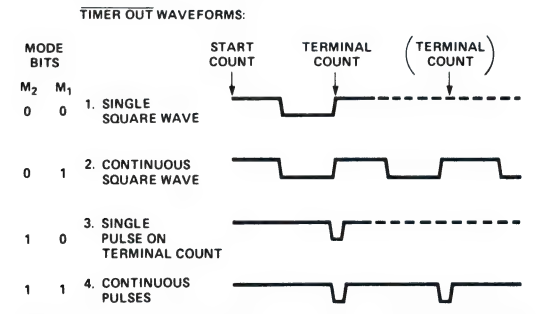


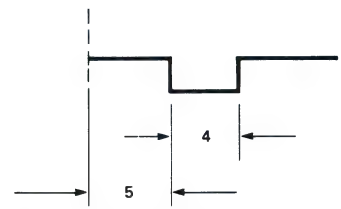
Figure 8. Timer Modes

Bits 6-7 (TM_2 and TM_1) of command register contents are used to start and stop the counter. There are four commands to choose from:

TM_2	TM_1	
0	0	NOP — Do not affect counter operation.
0	1	STOP — NOP if timer has not started; stop counting if the timer is running.
1	0	STOP AFTER TC — Stop immediately after present TC is reached (NOP if timer has not started)
1	1	START — Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached.

Note that while the counter is counting, you may load a new count and mode into the count length registers. Before the new count and mode will be used by the counter, you must issue a START command to the counter. This applies even though you may only want to change the count and use the previous mode.

In case of an odd-numbered count, the first half-cycle of the squarewave output, which is high, is one count longer than the second (low) half-cycle, as shown in Figure 9.



NOTE: 5 AND 4 REFER TO THE NUMBER OF CLOCKS IN THAT TIME PERIOD

Figure 9. Asymmetrical Square-Wave Output Resulting from Count of 9

The counter in the M8155 is not initialized to any particular mode or count when hardware RESET occurs, but RESET does *stop* the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

Please note that the timer circuit on the M8155 chip is designed to be a square-wave timer, not an event counter. To achieve this, it counts down by twos twice in completing one cycle. Thus, its registers do not contain values directly representing the number of TIMER IN pulses received. You cannot load an initial value of 1 into the count register and cause the timer to operate, as its terminal count value is 10 (binary) or 2 (decimal). (For the detection of single pulses, it is suggested that one of the hardware interrupt pins on the 8085A be used.) After the timer has started counting down, the values residing in the count registers can be used to calculate the actual number of TIMER IN pulses required to complete the timer cycle if desired. To obtain the remaining count, perform the following operations in order:

1. Stop the count
2. Read in the 16-bit value from the count length registers
3. Reset the upper two mode bits
4. Reset the carry and rotate right one position all 16 bits through carry
5. If carry is set, add 1/2 of the full original count (1/2 full count — 1 if full count is odd).

Note: If you started with an odd count and you read the count length register before the third count pulse occurs, you will not be able to discern whether one or two counts has occurred. Regardless of this, the M8155 always counts out the right number of pulses in generating the $\overline{\text{TIMER OUT}}$ waveforms.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS (T_A = -55°C to +125°C; V_{CC} = 5V ±10%)

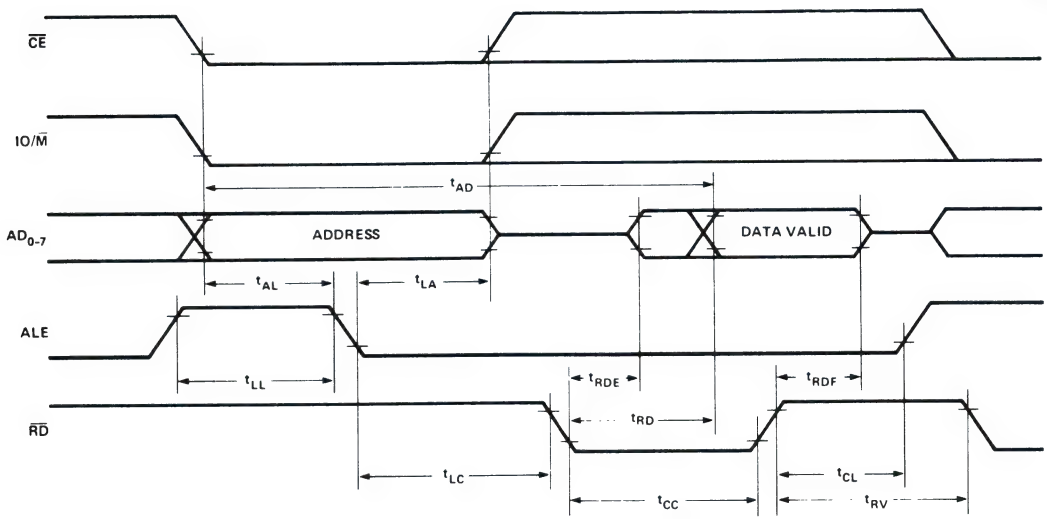
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} to 0V
I_{LO}	Output Leakage Current		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
I_{CC}	V_{CC} Supply Current		180	mA	
I_{IL}(CE)	Chip Enable Leakage M8155		+100	μA	V_{IN} = V_{CC} to 0V

A.C. CHARACTERISTICS (T_A = -55°C to +125°C; V_{CC} = 5V ±10%)

		M8155		
SYMBOL	**PARAMETER**	**MIN.**	**MAX.**	**UNITS**
t_{AL}	Address to Latch Set Up Time	50		ns
t_{LA}	Address Hold Time after Latch	80		ns
t_{LC}	Latch to READ/WRITE Control	100		ns
t_{RD}	Valid Data Out Delay from READ Control		170	ns
t_{AD}	Address Stable to Data Out Valid		400	ns
t_{LL}	Latch Enable Width	100		ns
t_{RDF}	Data Bus Float After READ	0	100	ns
t_{CL}	READ/WRITE Control to Latch Enable	20		ns
t_{CC}	READ/WRITE Control Width	250		ns
t_{DW}	Data In to WRITE Set Up Time	150		ns
t_{WD}	Data In Hold Time After WRITE	0		ns
t_{RV}	Recovery Time Between Controls	300		ns
t_{WP}	WRITE to Port Output		400	ns
t_{PR}	Port Input Setup Time	70		ns
t_{RP}	Port Input Hold Time	50		ns
t_{SBF}	Strobe to Buffer Full		400	ns
t_{SS}	Strobe Width	200		ns
t_{RBE}	READ to Buffer Empty		400	ns
t_{SI}	Strobe to INTR On		400	ns
t_{RDI}	READ to INTR Off		400	ns
t_{PSS}	Port Setup Time to Strobe Strobe	50		ns
t_{PHS}	Port Hold Time After Strobe	120		ns
t_{SBE}	Strobe to Buffer Empty		400	ns
t_{WBF}	WRITE to Buffer Full		400	ns
t_{WI}	WRITE to INTR Off		400	ns
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low		400	ns
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ High		400	ns
t_{RDE}	Data Bus Enable from READ Control	10		ns
t_1	TIMER-IN Low Time	80		ns
t_2	TIMER-IN High Time	120		ns

WAVEFORMS

a. Read Cycle



b. Write Cycle

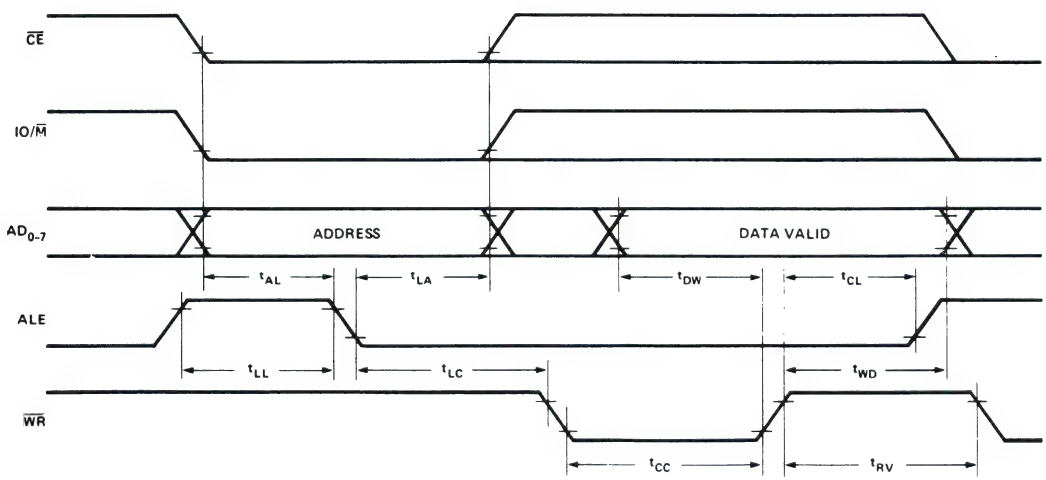
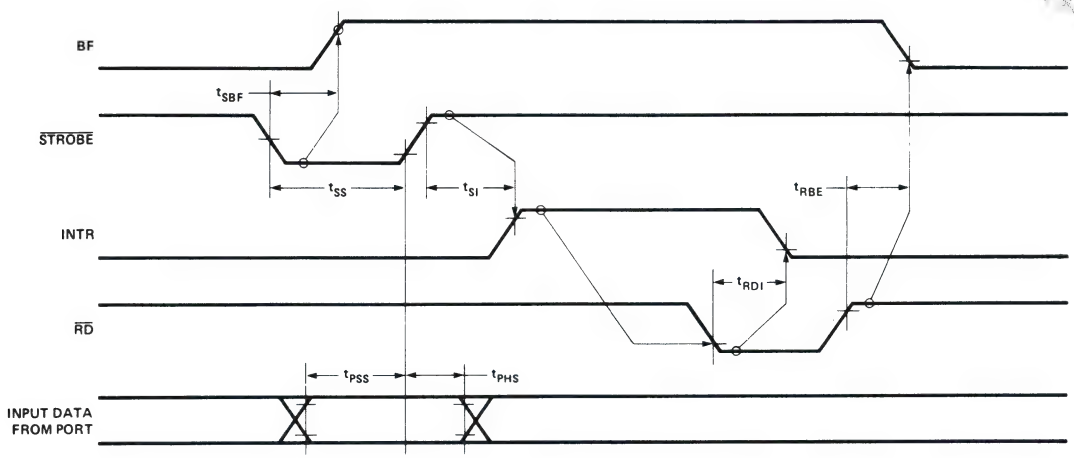


Figure 10. M8155 Read/Write Timing Diagrams

a. Strobed Input Mode



b. Strobed Output Mode

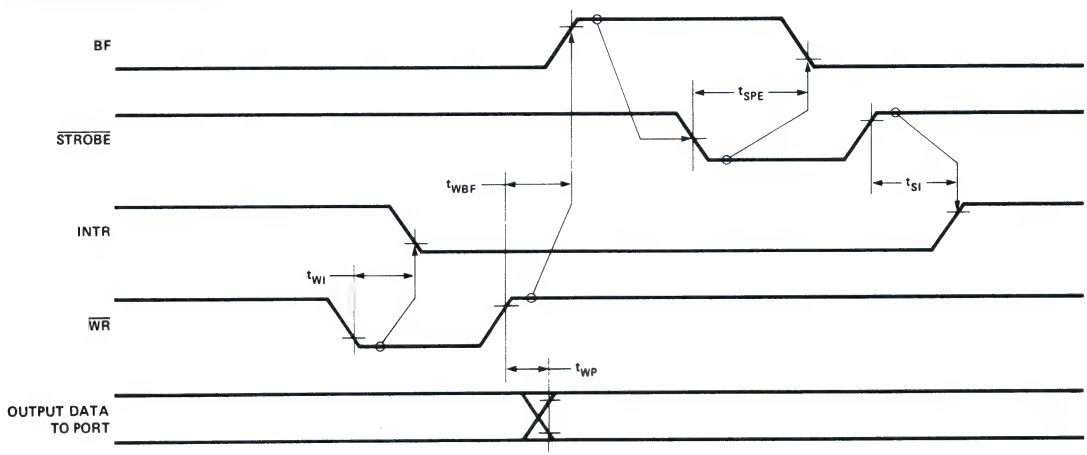
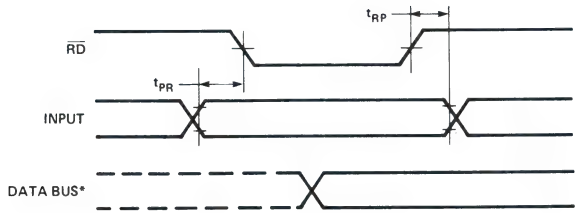
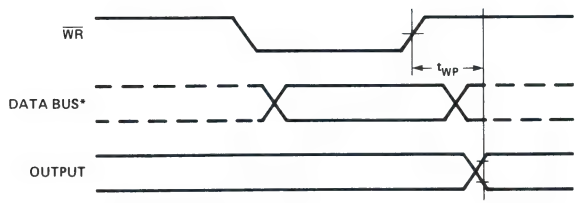


Figure 11. Strobed I/O Timing

a. Basic Input Mode

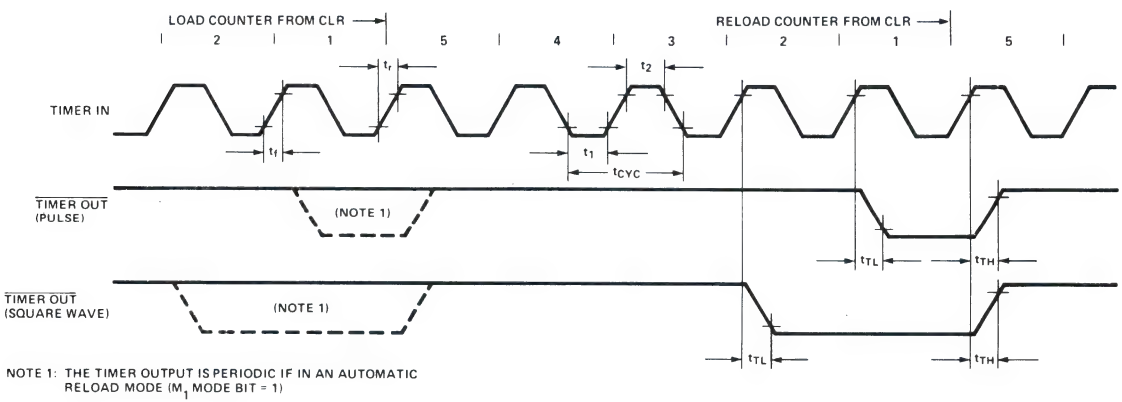


b. Basic Output Mode



*DATA BUS TIMING IS SHOWN IN FIGURE 7.

Figure 12. Basic I/O Timing Wavefore



NOTE 1: THE TIMER OUTPUT IS PERIODIC IF IN AN AUTOMATIC RELOAD MODE (M_1 MODE BIT = 1)

Figure 13. Timer Output Waveform Countdown from 5 to 1

M8755A
16,384-BIT EPROM WITH I/O

***Directly Compatible with M8085A CPU**

MILITARY

- **Military Temperature Range (−55°C to +100°C)**
- **2048 Words × 8 Bits**
- **Single +5V Power Supply (V_{CC})**
- **U.V. Erasable and Electrically Reprogrammable**
- **Internal Address Latch**
- **2 General Purpose 8-Bit I/O Ports**
- **Each I/O Port Line Individually Programmable as Input or Output**
- **Multiplexed Address and Data Bus**
- **40-Pin DIP**

The Intel® M8755A is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the MCS-85™ microcomputer system. The EPROM portion is organized as 2048 words by 8 bits.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is individually programmable as input or output.

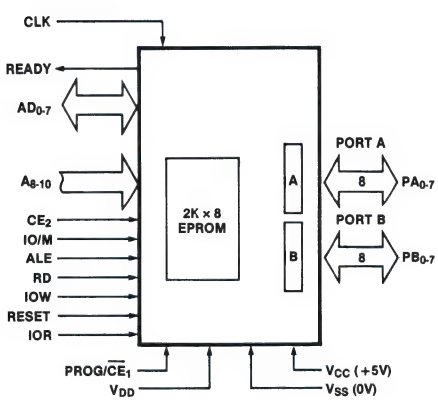


Figure 1. Block Diagram

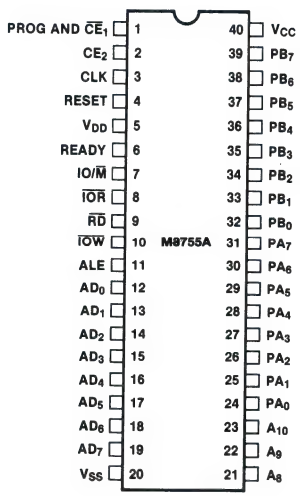


Figure 2. Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −55°C to +100°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation 1.5W

*Except for programming voltage

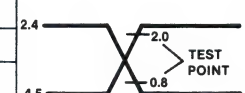
NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS ($T_A = -55°C$ to $+100°C$; $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.7	V	
V_{IH}	Input High Voltage	2.2	$V_{CC}+0.5$	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 1.6$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\ \mu A$
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{CC}$ to 0V
I_{LO}	Output Leakage Current		±10	μA	$0.45V \leqslant V_{OUT} \leqslant V_{CC}$
I_{CC}	V_{CC} Supply Current		220	mA	

A.C. CHARACTERISTICS ($T_A = -55°C$ to $100°C$; $V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{CYC}	Clock Cycle Time	320		ns	$C_{LOAD} = 150$ pF (See Figure 3)
T_1	CLK Pulse Width	80		ns	
T_2	CLK Pulse Width	120		ns	
t_f, t_r	CLK Rise and Fall Time		30	ns	
t_{AL}	Address to Latch Set Up Time	70		ns	150 pF Load
t_{LA}	Address Hold Time after Latch	100		ns	
t_{LC}	Latch to READ/WRITE Control	130		ns	
t_{RD}	Valid Data Out Delay from READ Control		300	ns	
t_{AD}	Address Stable to Data Out Valid		750	ns	
t_{LL}	Latch Enable Width	140		ns	
t_{RDF}	Data Bus Float after READ	0	100	ns	
t_{CL}	READ/WRITE Control to Latch Enable	50		ns	
t_{CC}	READ/WRITE Control Width	300		ns	
t_{DW}	Data In to WRITE Set Up Time	200		ns	
t_{WD}	Data In Hold Time After WRITE	100		ns	
t_{WP}	WRITE to Port Output		500	ns	
t_{PR}	Port Input Set Up Time	70		ns	
t_{RP}	Port Input Hold Time	70		ns	
t_{RYH}	READY HOLD TIME	0	220	ns	
t_{ARY}	ADDRESS (CE) to READY		160	ns	
t_{RV}	Recovery Time Between Controls	400		ns	
t_{RDE}	Data Out Delay from READ Control	20		ns	
t_{LD}	ALE to Data Out Valid		350	ns	Preliminary



M8086
16-BIT HMOS MICROPROCESSOR

- **Direct Addressing Capability to 1 MByte of Memory**
- **Assembly Language Compatible with 8080/8085**
- **14 Word, By 16-Bit Register Set with Symmetrical Operations**
- **24 Operand Addressing Modes**
- **Bit, Byte, Word, and Block Operations**
- **8-and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal Including Multiply and Divide**
- **5 MHz Clock Rate (8 MHz for 8086-2) (4 MHz for 8086-4)**
- **MULTIBUS™ System Compatible Interface**
- **Full Military Temperature Range −55°C to +125°C**

The Intel® M8086 is a new generation, high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The processor has attributes of both 8- and 16-bit microprocessors. It addresses memory as a sequence of 8-bit bytes, but has a 16-bit wide physical path to memory for high performance.

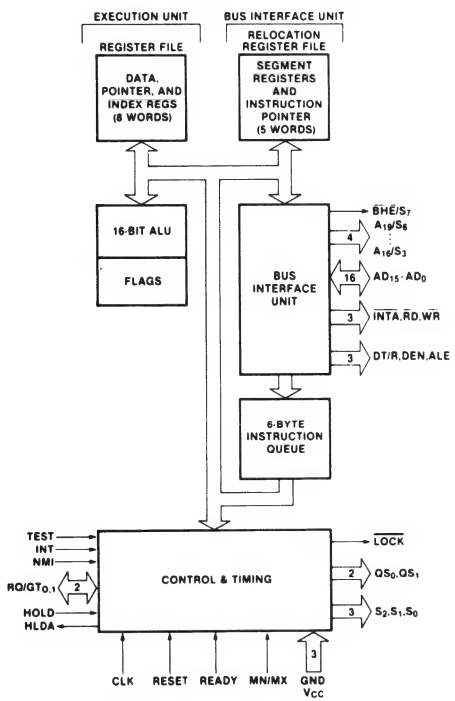
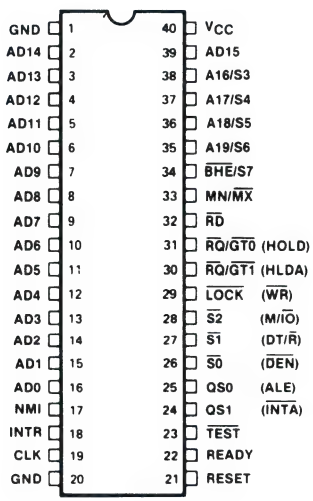


Figure 1. M8086 CPU Functional Block Diagram



40 LEAD

Figure 2. M8086 Pin Diagram

AUGUST 1979

A.C. CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$

8086 MINIMUM COMPLEXITY SYSTEM (Figures 8, 9, 12, 15)
TIMING REQUIREMENTS

		8086			
Symbol	**Parameter**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCLCL	CLK Cycle Period — 8086	200	500	ns	
TCLCH	CLK Low Time	(2/3 TCLCL)-15		ns	
TCHCL	CLK High Time	(1/3 TCLCL)+2		ns	
TCH1CH2	CLK Rise Time		10	ns	From 1.0V to 35.V
TCL2CL1	CLK Fall Time		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	30		ns	
TCLDX	Data In Hold Time	10		ns	
TR1VCL	RDY Setup Time into 8284 (See Notes 1, 2)	35		ns	
TCLR1X	RDY Hold Time into 8284 (See Notes, 1, 2)	0		ns	
TRYHCH	READY Setup Time Into 8086	(2/3 TCLCL)-15		ns	
TCHRYX	READY Hold Time Into 8086	30		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	-8		ns	
THVCH	HOLD Setup Time	35		ns	
TINVCH	INTR, NMI, $\overline{TEST}$ Setup Time (See Note 2)	30		ns	

TIMING RESPONSES

		8086			
Symbol	**Parameter**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCLAV	Address Valid Delay	10	110	ns	
TCLAX	Address Hold Time	10		ns	
TCLAZ	Address Float Delay	TCLAX	80	ns	
TLHLL	ALE Width	TCLCH-20		ns	
TCLLH	ALE Active Delay		80	ns	
TCHLL	ALE Inactive Delay		85	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL-10		ns	
TCLDV	Data Valid Delay	10	110	ns	$C_L = 20$-100 pF for all 8086 Outputs (In addition to 8086 self-load)
TCHDX	Data Hold Time	10		ns	
TWHDX	Data Hold Time After WR	TCLCH-30		ns	
TCVCTV	Control Active Delay 1	10	110	ns	
TCHCTV	Control Active Delay 2	10	110	ns	
TCVCTX	Control Inactive Delay	10	110	ns	
TAZRL	Address Float to READ Active	0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	165	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	150	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL-45		ns	
TCLHAV	HLDA Valid Delay	10	160	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL-75		ns	
TWLWH	$\overline{WR}$ Width	2TCLCL-60		ns	
TAVAL	Address Valid to ALE Low	TCLCH-60		ns	

NOTES: 1. Signal at 8284 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state (8 ns into T3).

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to Ground . . . . . −1.0 to +7V
Power Dissipation . . . . . 2.5 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC}+0.5$	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.0$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\ \mu A$
I_{CC}	Power Supply Current 8086/8086-4 8086-2		 340 350	 mA mA	$T_A = 25°C$
I_{LI}	Input Leakage Current		±10	μA	$0V < V_{IN} < V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0.45V \leqslant V_{OUT} \leqslant V_{CC}$
V_{CL}	Clock Input Low Voltage	−0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	$V_{CC}+1.0$	V	
C_{IN}	Capacitance of Input Buffer (All input except AD_0-AD_{15}, $\overline{RQ}/\overline{GT}$)		10	pF	fc = 1 MHz
C_{IO}	Capacitance of I/O Buffer (AD_0-AD_{15}, $\overline{RQ}/\overline{GT}$)		20	pF	fc = 1 MHz

M8282/8283
OCTAL LATCH

MILITARY

- **Fully Parallel 8-Bit Data Register and Buffer**
- **Transparent during Active Strobe**
- **Supports 8080, 8085, 8048, and 8086 Systems**
- **High Output Drive Capability for Driving System Data Bus**
- **3-State Outputs**
- **20-Pin Package with 0.3" Center**
- **No Output Low Noise when Entering or Leaving High Impedance State**
- **Full Military Temperature Range −55° to +125°C**

The M8282 and M8283 are 8-bit bipolar latches with 3-state output buffers. They can be used to implement latches, buffers, or multiplexers. The M8283 inverts the input data at its outputs while the M8282 does not. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with these devices.

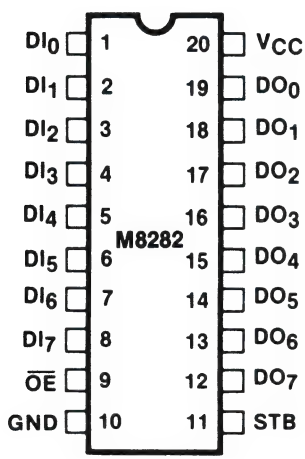


Figure 1. M8282 Pin Diagram

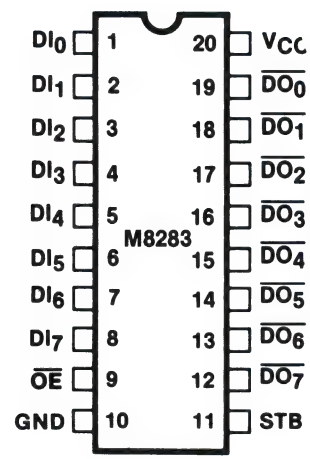


Figure 2. M8283 Pin Diagram

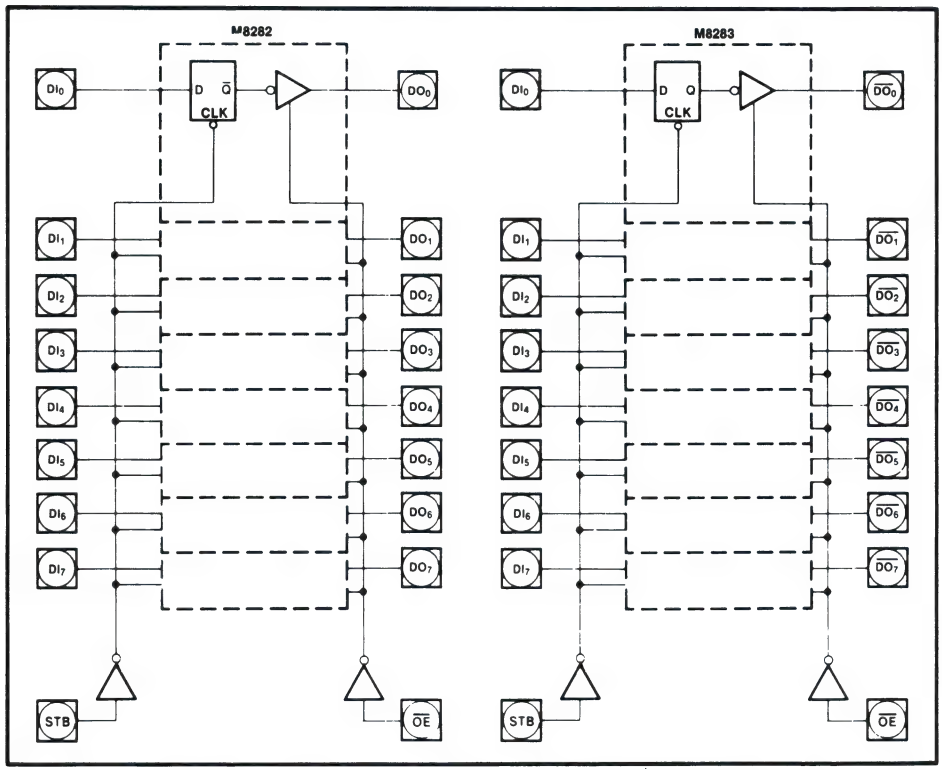


Figure 3. Logic Diagrams

PIN DEFINITIONS

Pin	Description
STB	STROBE (Input). STB is an input control pulse used to strobe data at the data input pins (A_0-A_7) into the data latches. This signal is active HIGH to admit input data. The data is latched at the HIGH to LOW transition of STB.
$\overline{OE}$	OUTPUT ENABLE (Input). $\overline{OE}$ is an input control signal which when active LOW enables the contents of the data latches onto the data output pin (B_0-B_7). $\overline{OE}$ being inactive HIGH forces the output buffers to their high impedance state.
DI_0-DI_7	DATA INPUT PINS (Input). Data presented at these pins satisfying setup time requirements when STB is strobed is latched into the data input latches.
DO_0-DO_7 (M8282) $\overline{DO_0}$-$\overline{DO_7}$ (M8283)	DATA OUTPUT PINS (Output). When $\overline{OE}$ is true, the data in the data latches is presented as inverted (M8283) or non-inverted (M8282) data onto the data output pins.

OPERATIONAL DESCRIPTION

The M8282 and M8283 octal latches are 8-bit latches with 3-state output buffers. Data having satisfied the setup time requirements is latched into the data latches by strobing the STB line HIGH to LOW. Holding the STB line in its active HIGH state makes the latches appear transparent. Data is presented to the data output pins by activating the $\overline{OE}$ input line. When $\overline{OE}$ is inactive HIGH the output buffers are in their high impedance state. Enabling or disabling the output buffers will not cause negative-going transients to appear on the data output bus.

D.C. AND A.C. OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
All Output and Supply Voltages ..... −0.5V to +7V
All Input Voltages ..... −1.0V to +5.5V
Power Dissipation ..... 1 Watt

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS FOR M8282/8283

Conditions: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $+125°C$

Symbol	Parameter	Min	Max	Units	Test Conditions
V_C	Input Clamp Voltage		−1	V	$I_C = -5$ mA
I_{CC}	Power Supply Current		160	mA	
I_F	Forward Input Current		−0.2	mA	$V_F = 0.45V$
I_R	Reverse Input Current		50	μA	$V_R = 5.25V$
V_{OL}	Output Low Voltage		.45	V	$I_{OL} = 32$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -5$ mA
I_{OFF}	Output Off Current		±50	μA	$V_{OFF} = 0.45$ to $5.25V$
V_{IL}	Input Low Voltage		0.8	V	$V_{CC} = 5.0V$ See Note 1
V_{IH}	Input High Voltage	2.0		V	$V_{CC} = 5.0V$ See Note 1
C_{IN}	Input Capacitance		12	pF	F = 1 MHz $V_{BIAS} = 2.5V$, $V_{CC} = 5V$ $T_A = 25°C$

Notes: 1. Output Loading $I_{OL} = 32$ mA, $I_{OH} = -5$ mA, $C_L = 300$ pF

A.C. CHARACTERISTICS FOR M8282/8283

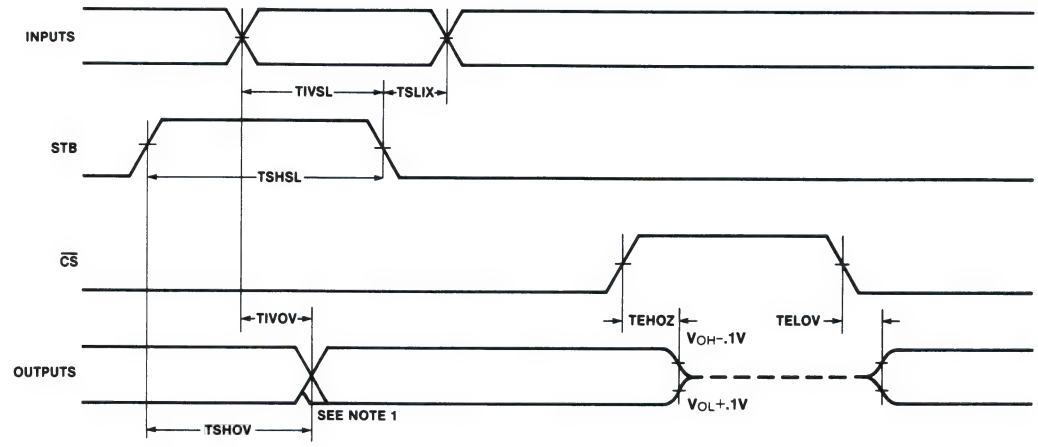
Conditions: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $+125°C$

Loading: Outputs — $I_{OL} = 32$ mA, $I_{OH} = -5$ mA, $C_L = 300$ pF

Symbol	Parameter	Min	Max	Units	Test Conditions
TIVOV	Input to Output Delay —Inverting —Non-Inverting		 22 30	 ns ns	(See Note 1)
TSHOV	STB to Output Delay —Inverting —Non-Inverting		 40 45	 ns ns	
TEHOZ	Output Disable Time		18	ns	
TELOV	Output Enable Time	10	30	ns	
TIVSL	Input to STB Setup Time	0		ns	
TSLIX	Input to STB Hold Time	25		ns	
TSHSL	STB High Time	15		ns	

NOTE: 1. See waveforms and test load circuit on following page.

M8282/8283 TIMING



NOTE: 1. 8283 ONLY — OUTPUT MAY BE MOMENTARILY INVALID FOLLOWING THE HIGH GOING STB TRANSITION.
2. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

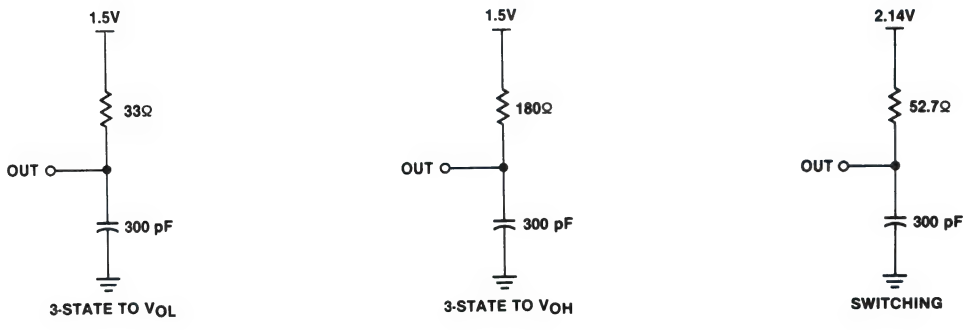


Figure 4. Output Test Load Circuits

M8284
CLOCK GENERATOR AND DRIVER FOR M8086 MICROPROCESSOR

- **Full Military Temperature Range: −55°C to +125°C**
- **Generates the System Clock for the M8086**
- **Uses a Crystal or TTL Signal for Frequency Source**
- **Single +5V Power Supply**
- **18-Pin Package**
- **Generates System Reset Output from Schmitt Trigger Input**
- **Provides Local Ready and MULTIBUS™ Ready Synchronization**
- **Capable of Clock Synchronization with other M8284's**

The M8284 is a bipolar clock generator/driver designed to provide clock signals for the M8086 and peripherals. It also contains READY logic for operation with two MULTIBUS™ systems and provides the processors required READY synchronization and timing. Reset logic with hysteresis and synchronization is also provided.

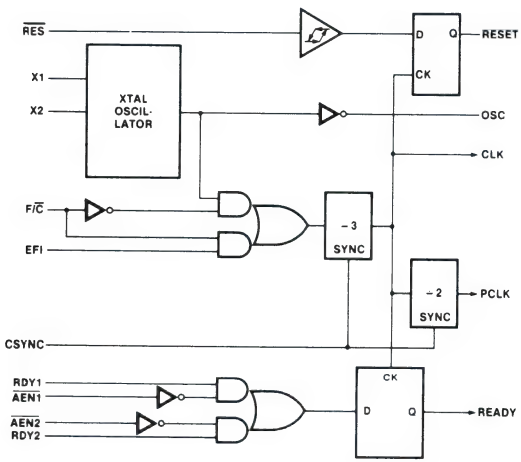


Figure 1. M8284 Block Diagram

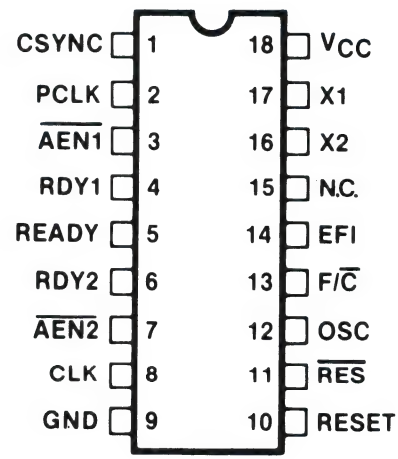


Figure 2. M8284 Pin Configuration

X1, X2	CONNECTIONS FOR CRYSTAL	RES	RESET INPUT
F/C	CLOCK SOURCE SELECT	RESET	SYNCHRONIZED RESET OUTPUT
EFI	EXTERNAL CLOCK INPUT	OSC	OSCILLATOR OUTPUT
CSYNC	CLOCK SYNCHRONIZATION INPUT	CLK	MOS CLOCK ID8086
RDY1, RDY2	READY SIGNAL FROM TWO MULTIBUS™ SYSTEMS	PCLK	TTL CLOCK FOR PERIPHERALS
AEN1, AEN2	ADDRESS ENABLED QUALIFIERS FOR RDY1,2	READY	SYNCHRONIZED READY OUTPUT
		VCC	+5 VOLTS
		GND	0 VOLTS

M8284 Pin Names

D.C. AND A.C. CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −55°C to 125°C
Storage Temperature ..... −65°C to +150°C
All Output and Supply Voltages..... −0.5V to +7V
All Input Voltages..... −1.0V to +5.5V
Power Dissipation.....1 Watt

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

Conditions: $T_A = -55°C$ to $125°C$; $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min	Max	Units	Test Conditions
I_F	Forward Input Current		−0.5	mA	$V_F = 0.45V$
I_R	Reverse Input Current		50	μA	$V_R = 5.25V$
V_C	Input Forward Clamp Voltage		−1.0	V	$I_C = -5$ mA
I_{CC}	Power Supply Current		140	mA	
V_{IL}	Input LOW Voltage		0.8	V	$V_{CC} = 5.0V$
V_{IH}	Input HIGH Voltage	2.0		V	$V_{CC} = 5.0V$
V_{IH_R}	Reset Input HIGH Voltage	2.6		V	$V_{CC} = 5.0V$
V_{OL}	Output LOW Voltage		0.45	V	5 mA
V_{OH}	Output HIGH Voltage CLK Other Outputs	4 2.4		V V	−1 mA −1 mA
V_{IH_R}-V_{IL_R}	$\overline{RES}$ Input Hysteresis	0.25		V	$V_{CC} = 5.0V$

A.C. CHARACTERISTICS

Conditions: $T_A = -55°C$ to $125°C$; $V_{CC} = 5V \pm 10\%$

TIMING REQUIREMENTS

Symbol	Parameter	Min	Max	Units	Test Conditions
TEHEL	External Frequency High Time	13		ns	90% - 90% V_{IN}
TELEH	External Frequency Low Time	13		ns	10% - 10% V_{IN}
TELEL	EFI Period	TEHEL + TELEH + δ		ns	(Note 1)
	XTAL Frequency	12	25	MHz	
TR1VCL	RDY1, RDY2 Set-Up to CLK	35		ns	
TCLR1X	RDY1, RDY2 Hold to CLK	0		ns	
TA1VR1V	$\overline{AEN1}$, $\overline{AEN2}$ Set-Up to RDY1, RDY2	15		ns	
TCLA1X	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	0		ns	
TYHEH	CSYNC Set-Up to EFI	20		ns	
TEHYL	CSYNC Hold to EFI	20		ns	
TYHYL	CSYNC Width	2·TELEL		ns	
TI1HCL	$\overline{RES}$ Set-Up to CLK	65		ns	(Note 2)
TCLI1H	$\overline{RES}$ Hold to CLK	20		ns	(Note 2)

M8286/8287
OCTAL BUS TRANSCEIVER

MILITARY

- **Data Bus Buffer Driver for MCS-86™, MCS-80™, MCS-85™, and MCS-48™ Families**
- **High Output Drive Capability for Driving System Data Bus**
- **Fully Parallel 8-Bit Transceivers**
- **3-State Outputs**
- **20-Pin Package with 0.3" Center**
- **No Output Low Noise when Entering or Leaving High Impedance State**
- **Full Military Temperature Range −55° to +125°C**

The M8286 and M8287 are 8-bit bipolar transceivers with 3-state outputs. The M8287 inverts the input data at is outputs while the M8286 does not. Thus, a wide variety of applications for buffering in microcomputer systems can be met.

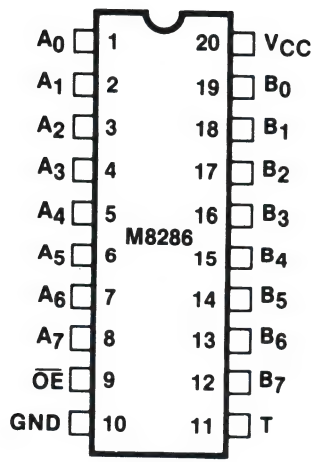


Figure 1. M8286 Pin Diagram

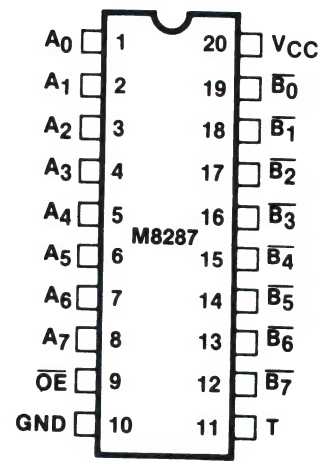


Figure 2. Pin Diagram

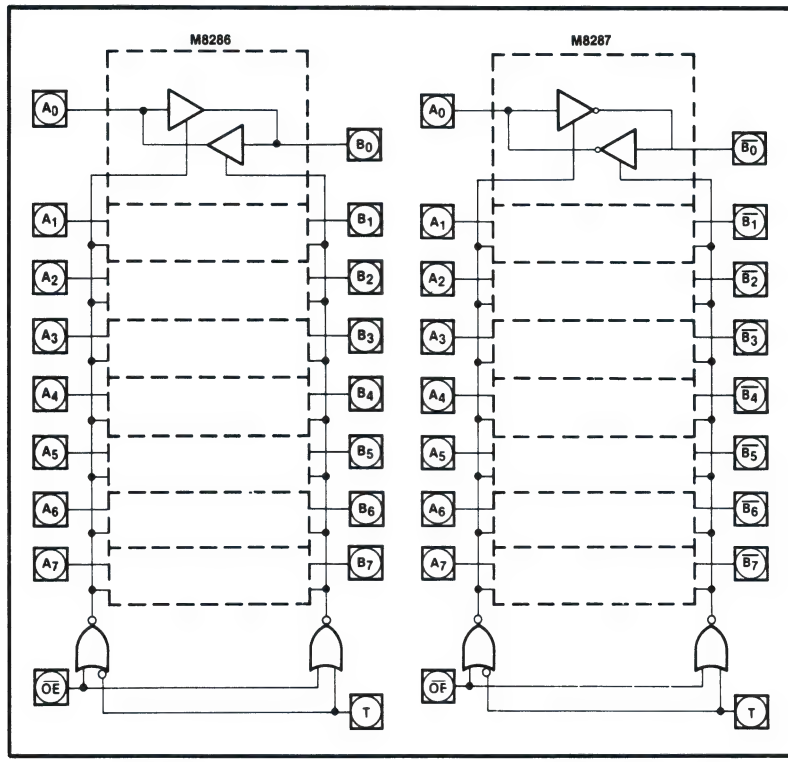


Figure 3. Logic Diagrams

PIN DEFINITIONS

Pin	Description
T	TRANSMIT (Input). T is an input control signal used to control the direction of the transceivers. When HIGH, it configures the transceiver's B_0-B_7 as outputs with A_0-A_7 as inputs. T LOW configures A_0-A_7 as the outputs with B_0-B_7 serving as the inputs.
$\overline{OE}$	OUTPUT ENABLE (Input). $\overline{OE}$ is an input control signal used to enable the appropriate output driver (as selected by T) onto its respective bus. This signal is active LOW.
A_0-A_7	LOCAL BUS DATA PINS (Input/Output). These pins serve to either present data to or accept data from the processor's local bus depending upon the state of the T pin.
B_0-B_7 (M8286) $\overline{B_0}$-$\overline{B_7}$ (M8287)	SYSTEM BUS DATA PINS (Input/Output). These pins serve to either present data to or accept data from the system bus depending upon the state of the T pin.

OPERATIONAL DESCRIPTION

The M8286 and M8287 transceivers are 8-bit transceivers with high impedance outputs. With T active HIGH and $\overline{OE}$ active LOW, data at the A_0-A_7 pins is driven onto the B_0-B_7 pins. With T inactive LOW and $\overline{OE}$ active LOW data at the B_0-B_7 pins is driven onto the A_0-A_7 pins. No output low glitching will occur whenever the transceivers are entering or leaving the high impedance state.

D.C. CHARACTERISTICS FOR M8286/8287

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
All Output and Supply Voltages ..... −0.5V to +7V
All Input Voltages ..... −1.0V to +5.5V
Power Dissipation ..... 1 Watt

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS FOR 8286/8287

Conditions: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $+125°C$

Symbol	Parameter	Min	Max	Units	Test Conditions
V_C	Input Clamp Voltage		-1	V	$I_C = -5$ mA
I_{CC}	Power Supply Current—8287 —8286		130 160	mA mA	
I_F	Forward Input Current		-0.2	mA	$V_F = 0.45V$
I_R	Reverse Input Current		50	μA	$V_R = 5.25V$
V_{OL}	Output Low Voltage —B Outputs —A Outputs		.45 .45	V V	I_{OL} = 32 mA I_{OL} = 16 mA
V_{OH}	Output High Voltage —B Outputs —A Outputs	2.4 2.4		V V	$I_{OH} = -5$ mA $I_{OH} = -1$ mA
I_{OFF} I_{OFF}	Output Off Current Output Off Current		I_F I_R		$V_{OFF} = 0.45V$ $V_{OFF} = 5.25V$
V_{IL}	Input Low Voltage —A Side —B Side		0.8 0.9	V V	$V_{CC} = 5.0V$, See Note 1 $V_{CC} = 5.0V$, See Note 1
V_{IH}	Input High Voltage	2.0		V	$V_{CC} = 5.0V$, See Note 1
C_{IN}	Input Capacitance		12	pF	F = 1 MHz $V_{BIAS} = 2.5V$, $V_{CC} = 5V$ $T_A = 25°C$

Note: 1. B Outputs — I_{OL} = 32 mA, I_{OH} = -5 mA, C_L = 300 pF A Outputs — I_{OL} = 16 mA, I_{OH} = -1 mA, C_L = 100 pF

A.C. CHARACTERISTICS FOR M8286/8287

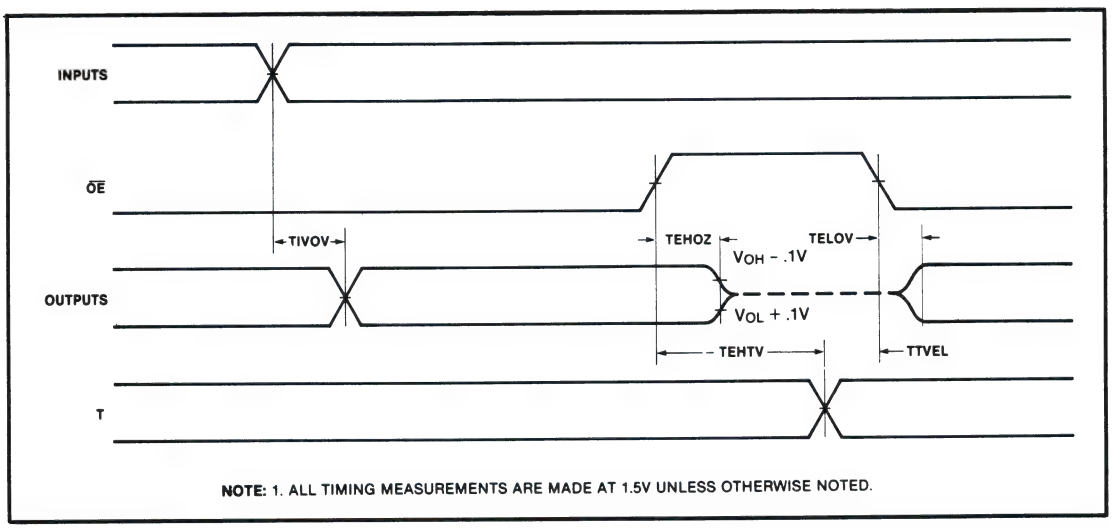
Conditions: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $+125°C$

Loading: B Outputs — I_{OL} = 32 mA, I_{OH} = -5 mA, C_L = 300 pF
A Outputs — I_{OL} = 16 mA, I_{OH} = -1 mA, C_L = 100 pF

Symbol	Parameter	Min	Max	Units	Test Conditions
TIVOV	Input to Output Delay Inverting Non-Inverting		 22 30	 ns ns	(See Note 1)
TEHTV	Transmit/Receive Hold Time	TEHOZ		ns	
TTVEL	Transmit/Receive Setup	30		ns	
TEHOZ	Output Disable Time		18	ns	
TELOV	Output Enable Time	10	30	ns	

Note: 1. See waveforms and test load circuit on following page.

M8286/8287 TIMING



NOTE: 1. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.

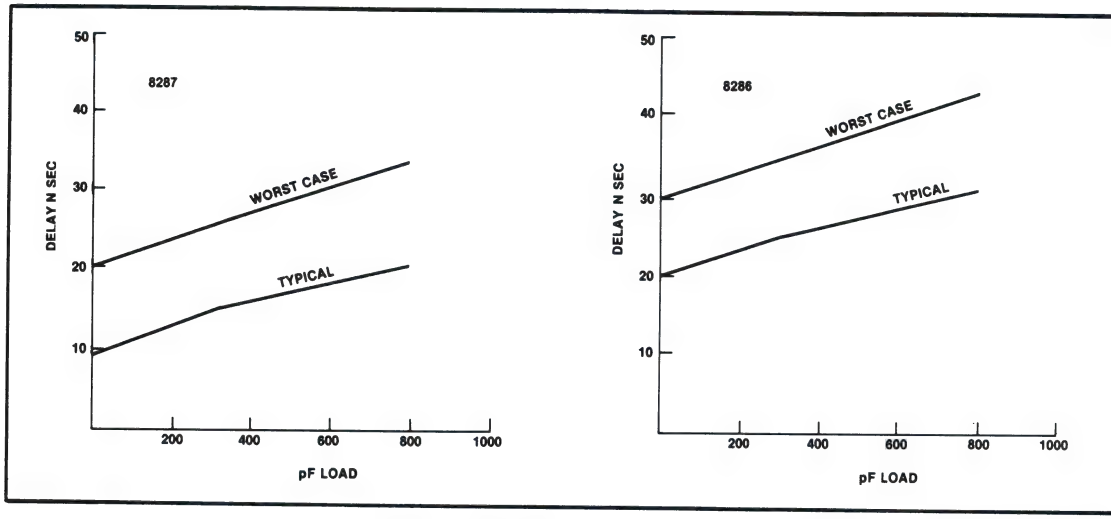


Figure 4. Output Delay vs. Capacitance

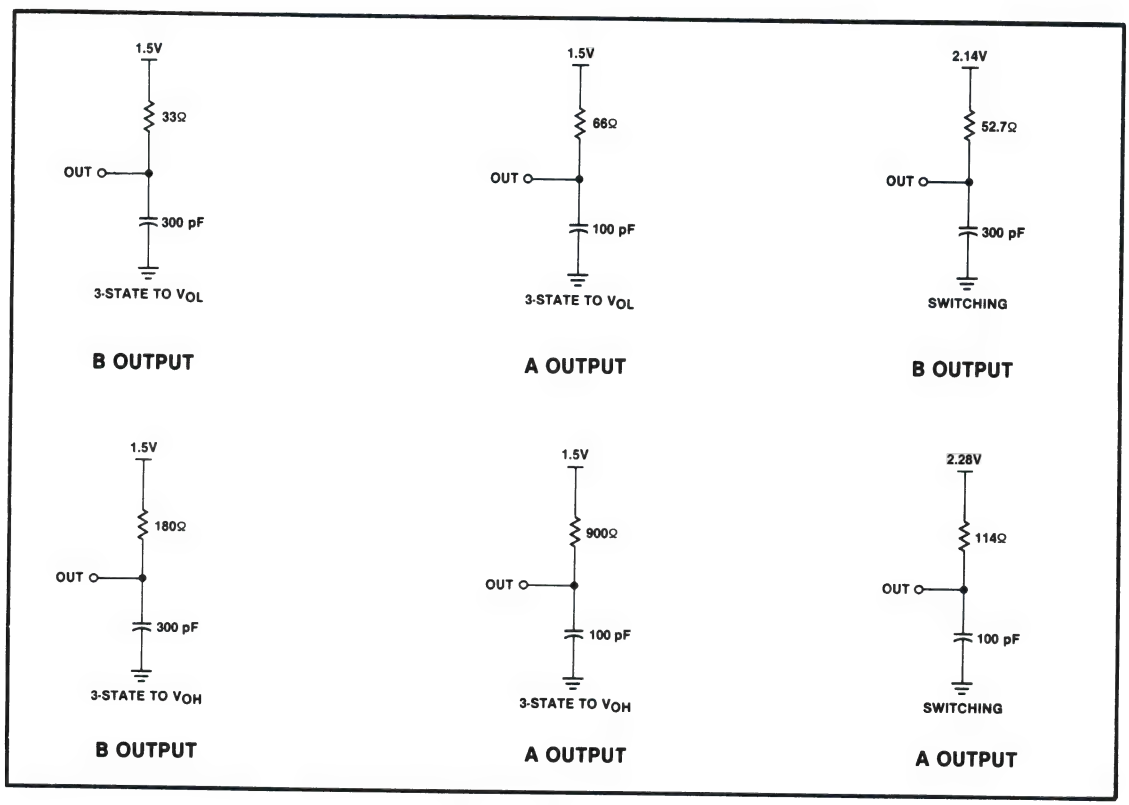


Figure 5. Test Load Circuits

M8288
BUS CONTROLLER
FOR M8086 MICROPROCESSOR

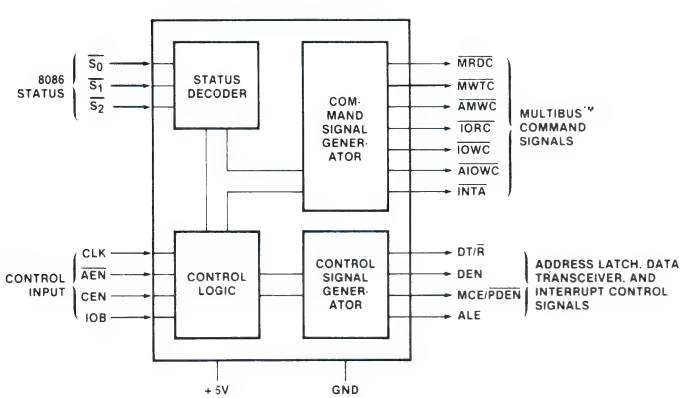
- **Bipolar Drive Capability**
- **3-State Command Output Drivers**
- **Provides Advanced Commands**
- **Configurable for Use with an I/O Bus**
- **Provides Wide Flexibility in System Configurations**
- **Facilitates Interface to One or Two Multi-Master Busses**

- **Military Temperature Range −55°C to +125°C**

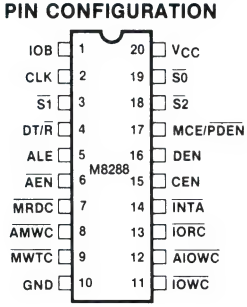
The Intel® M8288 Controller is a 20-pin bipolar component for use with medium-to-large 8086 processing systems. The bus controller provides command and control timing generation as well as bipolar bus drive capability while optimizing system performance.

A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.

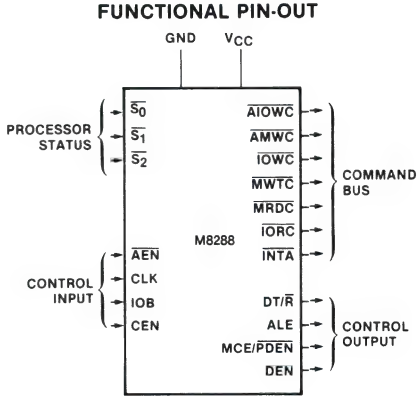
BLOCK DIAGRAM



PIN CONFIGURATION



FUNCTIONAL PIN-OUT



D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −55°C to 125°C
Storage Temperature ..... −65°C to +150°C
All Output and Supply Voltages ..... −0.5V to +7V
All Input Voltages ..... −1.0V to +5.5V
Power Dissipation ..... 1.5 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS FOR THE M8288

Conditions: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $125°C$

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_C	Input Clamp Voltage		−1	V	$I_C = -5$ mA
I_{CC}	Power Supply Current		230	mA	
I_F	Forward Input Current		−0.7	mA	$V_F = 0.45V$
I_R	Reverse Input Current		50	μA	$V_R = V_{CC}$
V_{OL}	Output Low Voltage—Command Outputs Control Outputs		0.5 0.5	V V	$I_{OL} = 20$ mA $I_{OL} = 16$ mA
V_{OH}	Output High Voltage—Command Outputs Control Outputs	2.4 2.4		V V	$I_{OH} = -5$ mA $I_{OH} = -1$ mA
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
I_{OFF}	Output Off Current		100	μA	$V_{OFF} = 0.4$ to $5.25V$

A.C. CHARACTERISTICS FOR THE M8288

Conditions: $V_{CC} = 5V \pm 10\%$, $T_A = -55°C$ to $125°C$

TIMING REQUIREMENTS

Symbol	Parameter	Min	Max	Unit	Loading
TCLCL	CLK Cycle Period	125		ns	
TCLCH	CLK Low Time	66		ns	
TCHCL	CLK High Time	40		ns	
TSVCH	Status Active Setup Time	65		ns	
TCHSV	Status Active Hold Time	10		ns	
TSHCL	Status Inactive Setup Time	55		ns	
TCLSH	Status Inactive Hold Time	10		ns	

TIMING RESPONSES

Symbol	Parameter	Min	Max	Unit	Loading
TCVNV	Control Active Delay	5	45	ns	
TCVNX	Control Inactive Delay	10	45	ns	
TCLLH, TCLMCH	ALE MCE Active Delay (from CLK)		15	ns	
TSVLH, TSVMCH	ALE MCE Active Delay (from Status)		25	ns	
TCHLL	ALE Inactive Delay		20	ns	$\overline{MRDC}$, $\overline{IORC}$, $\overline{MWTC}$, $\overline{IOWC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{AIOWC}$: $I_{OL} = 20$ mA, $I_{OH} = -5$ mA, $C_L = 300$ pF
TCLML	Command Active Delay	10	35	ns	
TCLMH	Command Inactive Delay	10	35	ns	
TCHDTL	Direction Control Active Delay		50	ns	
TCHDTH	Direction Control Inactive Delay		30	ns	
TAELCH	Command Enable Time		40	ns	
TAEHCZ	Command Disable Time		40	ns	
TAELCV	Enable Delay Time	105	275	ns	Other: $I_{OL} = 16$ mA, $I_{OH} = -1$ mA, $C_L = 80$ pF
TAEVNV	$\overline{AEN}$ to DEN		20	ns	
TCEVNV	CEN to DEN, PDEN		30	ns	
TCELRH	CEN to Command		TCLML	ns	

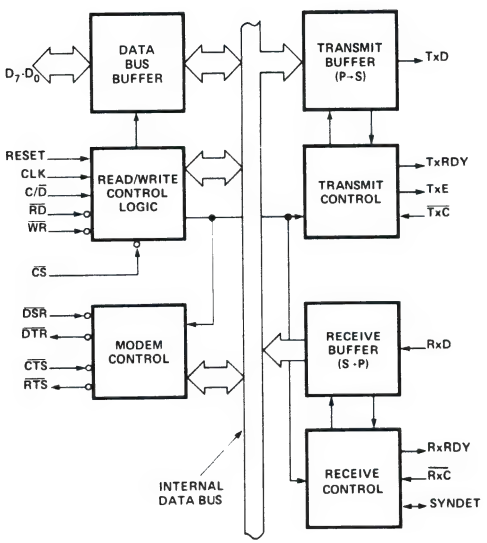
M8251A
PROGRAMMABLE COMMUNICATION INTERFACE

MILITARY

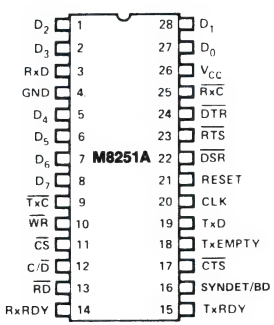
- **Synchronous and Asynchronous Operation**
- **Synchronous 5-8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion**
- **Asynchronous 5-8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling.**
- **Synchronous Baud Rate — DC to 64K Baud**
- **Military Temperature Range −55°C to +125°C**
- **Asynchronous Baud Rate — DC to 19.2K Baud**
- **Full Duplex, Double Buffered, Transmitter and Receiver**
- **Error Detection — Parity, Overrun and Framing**
- **Fully Compatible with M8080/M8085 CPU**
- **28-Pin DIP Package**
- **All Inputs and Outputs are TTL Compatible**
- **Single +5V Supply**
- **Single TTL Clock**

The Intel® M8251A is the enhanced version of the industry standard, Intel® 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's new high performance family of microprocessors such as the M8085. The M8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is constructed using N-channel silicon gate technology.

BLOCK DIAGRAM



PIN CONFIGURATION



FEATURES AND ENHANCEMENTS

8251A is an advanced design of the industry standard USART, the Intel® 8251. The M8251A operates with an extended range of Intel microprocessors that includes the new 8085 CPU and maintains compatibility with the 8251. Familiarization time is minimal because of compatibility and involves only knowing the additional features and enhancements and reviewing the AC and DC specifications of the M8251A.

The M8251A incorporates all the key features of the M8251 and has the following additional features and enhancements:

- M8251A has double-buffered data paths with separate I/O registers for control, status, Data In, and Data Out, which considerably simplifies control programming and minimizes CPU overhead.
- In asynchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
- A refined Rx initialization prevents the Receiver from starting when in "break" state, preventing unwanted interrupts from a disconnected USART.
- At the conclusion of a transmission, TxD line will always return to the marking state unless SBRK is programmed.
- Tx Enable logic enhancement prevents a Tx Disable command from halting transmission until all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.
- When External Sync Detect is programmed, Internal Sync Detect is disabled, and an External Sync Detect status is provided via a flip-flop which clears itself upon a status read.
- Possibility of false sync detect is minimized by ensuring that if double character sync is programmed, the characters be contiguously detected and also by clearing the Rx register to all ones whenever Enter Hunt command is issued in Sync mode.
- As long as the M8251A is not selected, the RD and $\overline{WR}$ do not affect the internal operation of the device.
- The M8251A Status can be read at any time but the status update will be inhibited during status read.
- The M8251A is free from extraneous glitches and has enhanced AC and DC characteristics, providing higher speed and better operating margins.
- Synchronous Baud rate from DC to 64K.
- Fully compatible with Intel's new industry standard, the MCS-85.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . −0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = −55°C to 125°C; V_{CC} = 5.0V ±5%; GND = 0V

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} TO 0.45V
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} TO 0.45V
I_{CC}	Power Supply Current		100	mA	All Outputs = High

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND

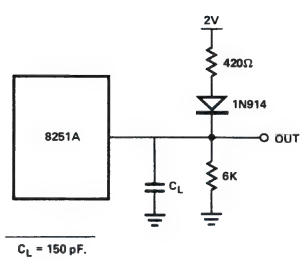


Figure 16. Test Load Circuit

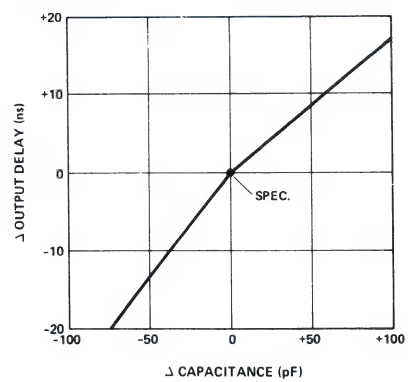


Figure 17. Typical Δ Output Delay vs. Δ Capacitance (pF)

A.C. CHARACTERISTICS

T_A = −55°C to 125°C; V_{CC} = 5.0V ±5%; GND = 0V

Bus Parameters (Note 1)

Read Cycle:

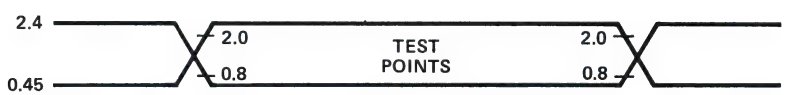
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	−75		ns	Note 2
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	75		ns	Note 2
t_{RR}	$\overline{READ}$ Pulse Width	300		ns	
t_{RD}	Data Delay from $\overline{READ}$		280	ns	3, C_L = 150 pF
t_{DF}	$\overline{READ}$ to Data Floating	5	120	ns	

Write Cycle:

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{AW}	Address Stable Before $\overline{WRITE}$	75		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	75		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	300		ns	
t_{DW}	Data Set Up Time for $\overline{WRITE}$	200		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	80		ns	
t_{RV}	Recovery Time Between WRITES	6		t_{CY}	Note 4

NOTES: 1. AC timings measured V_{OH} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.
2. Chip Select ($\overline{CS}$) and Command/Data (C/$\overline{D}$) are considered as Addresses.
3. Assumes that Address is valid before $\overline{RD}\downarrow$.
4. This recovery time is for Mode Initialization only. Write Data is allowed only when TxRDY = 1.
Recovery Time between Writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 16 t_{CY}.

Input Waveforms for AC Tests



Other Timings:

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_{CY}	Clock Period	320	1350	ns	Notes 5, 6
t_{ϕ}	Clock High Pulse Width	150	$t_{CY}-100$	ns	
$t_{\overline{\phi}}$	Clock Low Pulse Width	100		ns	
t_R, t_F	Clock Rise and Fall Time		20	ns	
t_{DTx}	TxD Delay from Falling Edge of $\overline{TxC}$		1	μs	
f_{Tx}	Transmitter Input Clock Frequency				
	1x Baud Rate	DC	64	kHz	
	16x Baud Rate	DC	310	kHz	
	64x Baud Rate	DC	615	kHz	
t_{TPW}	Transmitter Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1x Baud Rate	DC	64	kHz	
	16x Baud Rate	DC	310	kHz	
	64x Baud Rate	DC	615	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1x Baud Rate	12		t_{CY}	
	16x and 64x Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1x Baud Rate	15		t_{CY}	
	16x and 64x Baud Rate	3		t_{CY}	
t_{TxRDY}	TxRDY Pin Delay from Center of last Bit		8	t_{CY}	Note 7
$t_{TxRDY\ CLEAR}$	TxRDY ↓ from Leading Edge of $\overline{WR}$		6	t_{CY}	Note 7
t_{RxRDY}	RxRDY Pin Delay from Center of last Bit		24	t_{CY}	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY ↓ from Leading Edge of $\overline{RD}$		6	t_{CY}	Note 7
t_{IS}	Internal SYNDET Delay from Rising Edge of $\overline{RxC}$		24	t_{CY}	Note 7
t_{ES}	External SYNDET Set-Up Time Before Falling Edge of $\overline{RxC}$	16		t_{CY}	Note 7
$t_{TxEMPTY}$	TxEMPTY Delay from Center of Last Bit	20		t_{CY}	Note 7
t_{WC}	Control Delay from Rising Edge of WRITE (TxEn, $\overline{DTR}$, $\overline{RTS}$)	8		t_{CY}	Note 7
t_{CR}	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)	20		t_{CY}	Note 7

5. The TxC and RxC frequencies have the following limitations with respect to CLK.
   For 1x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
   For 16x and 64x Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$

6. Reset Pulse Width = 6 t_{CY} minimum; System Clock must be running during Reset.
7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

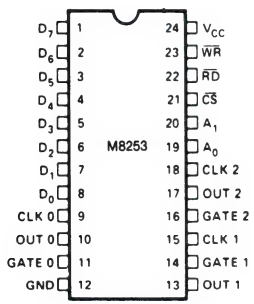
M8253
PROGRAMMABLE INTERVAL TIMER

- **3 Independent 16-Bit Counters**
- **Count Binary or BCD**
- **Full Military Temperature Range −55°C to +125°C**
- **Single +5V Supply**
- **Programmable Counter Modes**
- **24-Pin Dual In-Line Package**

The Intel® M8253 is a programmable counter/timer chip designed for use as an Intel microcomputer peripheral. It uses nMOS technology with a single −5V supply and is packaged in a 24-pin DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

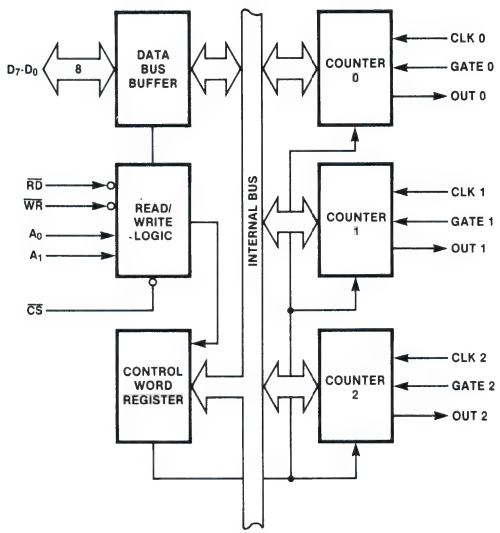
PIN CONFIGURATION



PIN NAMES

D_7 D_0	DATA BUS (8 BIT)
CLK N	COUNTER CLOCK INPUTS
GATE N	COUNTER GATE INPUTS
OUT N	COUNTER OUTPUTS
$\overline{RD}$	READ COUNTER
WR	WRITE COMMAND OR DATA
CS	CHIP SELECT
A_0 A_1	COUNTER SELECT
V_{CC}	+5 VOLTS
GND	GROUND

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5 V to +7 V
Power Dissipation ..... 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.2		V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −150 μA
I_{IL}	Input Load Current		±20	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±20	μA	V_{OUT} = V_{CC} to 0V
I_{CC}	V_{CC} Supply Current		160	mA	

CAPACITANCE T_A = 25°C; V_{CC} = GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = 5.0V ±5%; GND = 0V

Bus Parameters (Note 1)

Read Cycle:

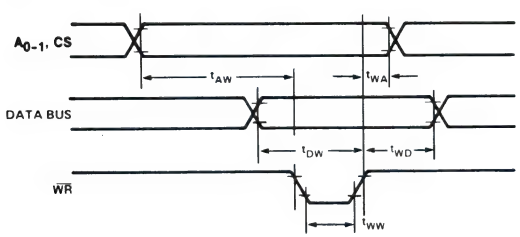
SYMBOL	PARAMETER	8253 MIN.	8253 MAX.	UNIT
t_{AR}	Address Stable Before $\overline{READ}$	50		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		ns
t_{RR}	$\overline{READ}$ Pulse Width	400		ns
t_{RD}	DATA Delay from $\overline{READ}$(2)		300	ns
t_{DF}	$\overline{READ}$ to Data Floating	25	125	ns
t_{RV}	Recovery Time Between $\overline{READ}$ and Any Other Control Signal	1		μs

Write Cycle:

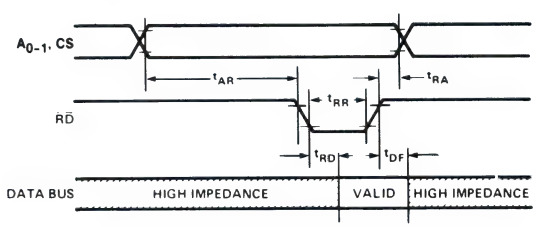
SYMBOL	PARAMETER	8253 MIN.	8253 MAX.	UNIT
t_{AW}	Address Stable Before $\overline{WRITE}$	50		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	30		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		ns
t_{RV}	Recovery Time Between $\overline{WRITE}$ and Any Other Control Signal	1		μs

Notes: 1. AC timings measured at V_{OH} = 2.4, V_{OL} = 0.8
2. Test Conditions: 8253, C_L = 100pF

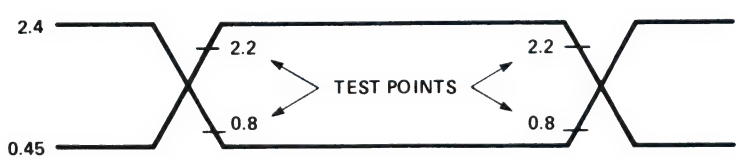
Write Timing:



Read Timing:



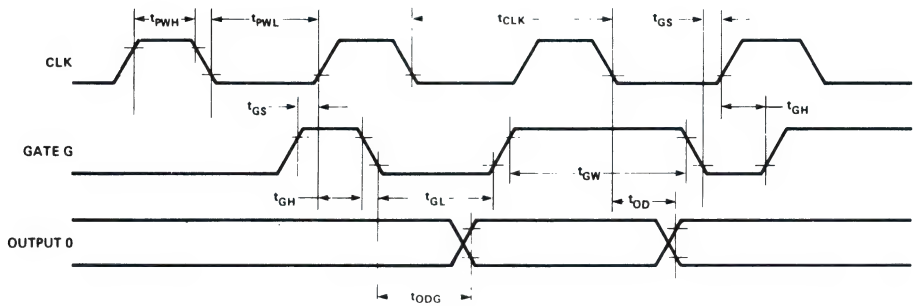
Input Waveforms for A.C. Tests:



Clock and Gate Timing:

SYMBOL	PARAMETER	8253		UNIT
		MIN.	MAX.	
t_{CLK}	Clock Period	380	dc	ns
t_{PWH}	High Pulse Width	230		ns
t_{PWL}	Low Pulse Width	150		ns
t_{GW}	Gate Width High	150		ns
t_{GL}	Gate Width Low	100		ns
t_{GS}	Gate Set Up Time to CLK↑	100		ns
t_{GH}	Gate Hold Time After CLK↑	50		ns
t_{OD}	Output Delay From CLK↓[1]		400	ns
t_{ODG}	Output Delay From Gate↓[1]		300	ns

Note 1: Test Conditions: C_L = 100pF.



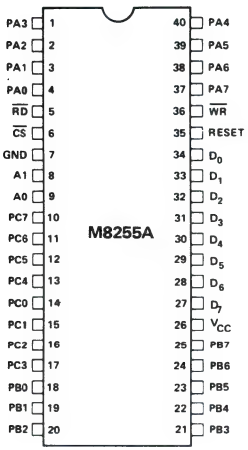
M8255A
PROGRAMMABLE PERIPHERAL INTERFACE

- **24 Programmable I/O Pins**
- **Completely TTL Compatible**
- **Fully Compatible with MCS-80™ Microprocessor Family**
- **Full Military Temperature Range −55°C to +125°C**
- **Direct Bit Set/Reset Capability Easing Control Application Interface**
- **40-Pin Dual In-Line Package**
- **Reduces System Package Count**
- **±10% Power Supply Tolerance**

The Intel® M8255A is a general purpose programmable I/O device designed for use with microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

Other features of the M8255A include bit set and reset capability and the ability to source 1 mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

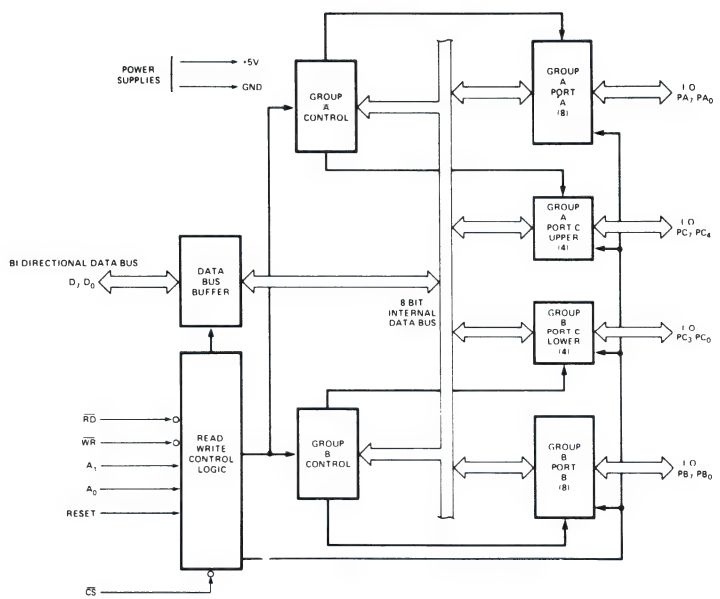
PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	Ø VOLTS

M8255A BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage On Any Pin
With Respect to GND . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 Watt

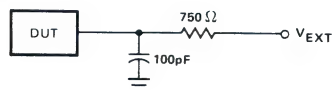
**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = -55°C to +125°C; V_{CC} = +5V ±10%; GND = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}	V	
V_{OL} (DB)	Output Low Voltage (Data Bus)		0.45	V	I_{OL} = 2.5mA
V_{OL}(PER)	Output Low Voltage (Peripheral Port)		0.45	V	I_{OL} = 1.7mA
V_{OH}(DB)	Output High Voltage (Data Bus)	2.4		V	I_{OH} = -400μA
V_{OH}(PER)	Output High Voltage (Peripheral Port)	2.4		V	I_{OH} = -200μA
I_{DAR}[1]	Darlington Drive Current	-1.0	-4.0	mA	
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V

Note 1: Available on any 8 pins from Port B and C.

TEST CIRCUIT



A.C. CHARACTERISTICS T_A = -55°C to +125°C, V_{CC} = +5V ±10%; GND = 0V

SYMBOL	PARAMETER	8255A MIN.	8255A MAX.	UNIT
t_{AR}	Address Stable Before READ	0		ns
t_{RA}	Address Stable After READ	0		ns
t_{RR}	READ Pulse Width	300		ns
t_{RD}	Data Valid From READ[1]		250	ns
t_{DF}	Data Float After READ	10	150	ns
t_{RV}	Time Between READs and/or WRITEs	850		ns
t_{AW}	Address Stable Before WRITE	0		ns
t_{WA}	Address Stable After WRITE	20		ns
t_{WW}	WRITE Pulse Width	400		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		ns
t_{WD}	Data Valid After WRITE	30		ns
t_{WB}	WR = 1 to Output[1]		350	ns
t_{IR}	Peripheral Data Before RD	0		ns
t_{HR}	Peripheral Data After RD	0		ns
t_{AK}	ACK Pulse Width	300		ns
t_{ST}	STB Pulse Width	500		ns
t_{PS}	Per. Data Before T.E. of STB	0		ns

A.C. CHARACTERISTICS (continued)

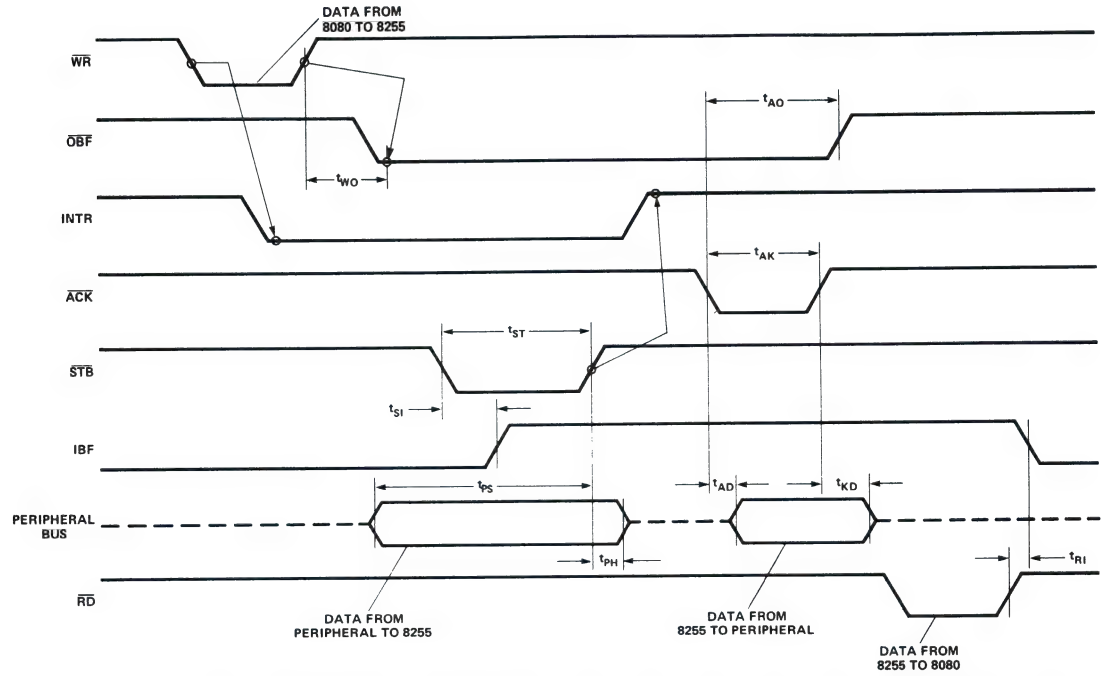
t_{PH}	Per. Data After T.E. of STB	180		ns
t_{AD}	ACK = 0 to Output[1]		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	ns
t_{WOB}	WR = 1 to OBF = 0[1]		650	ns
t_{AOB}	ACK = 0 to OBF = 1[1]		350	ns
t_{SIB}	STB = 0 to IBF = 1[1]		300	ns
t_{RIB}	RD = 1 to IBF = 0[1]		300	ns
t_{RIT}	RD = 0 to INTR = 0[1]		400	ns
t_{SIT}	STB = 1 to INTR = 1[1]		300	ns
t_{AIT}	ACK = 1 to INTR = 1[1]		350	ns
t_{WIT}	WR = 0 to INTR = 0[1]		850	ns

Notes:
1. Test condition: 8255A: C_L = 100pF
2. Period of Reset pulse must be at least 50μF during or after power on. Subsequent Reset pulse can be 500ns min.

CAPACITANCE T_A = 25°C, V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

TIMING DIAGRAM

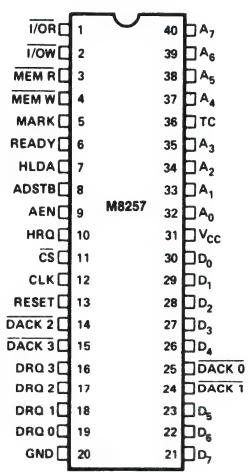


M8257
PROGRAMMABLE DMA CONTROLLER

- **Full Military Temp. Range −55°C to 125°C**
- **4-Channel DMA Controller**
- **Priority DMA Request Logic**
- **Channel Inhibit Logic**
- **Terminal Count and Modulo 128 Outputs**
- **Single TTL Clock**
- **Single +5V Supply**
- **Auto Load Mode**

The Intel® M8257 is a 4-channel direct memory access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for the Intel® microcomputer systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus in accomplished via the CPU's hold function. The M8257 has priority logic that resolves the peripherals requests and issues a composite hold request to the CPU. It maintains the DMA cycle count for each channel and outputs a control signal to notify the peripheral that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers. The M8257 represents a significant savings in component count for DMA-based microcomputer systems and greatly simplifies the transfer of data at high speed between peripherals and memories.

PIN CONFIGURATION

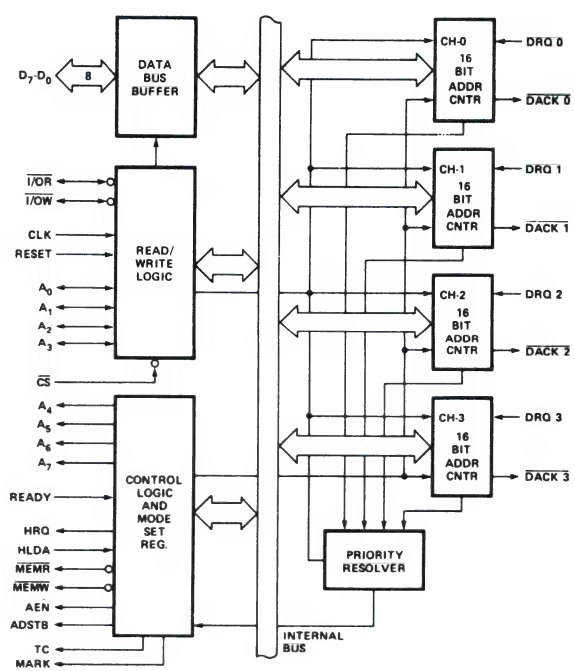


PIN NAMES

D_7-D_0	DATA BUS
A_7-A_0	ADDRESS BUS
$\overline{I/OR}$	I/O READ
$\overline{I/OW}$	I/O WRITE
$\overline{MEMR}$	MEMORY READ
$\overline{MEMW}$	MEMORY WRITE
CLK	CLOCK INPUT
RESET	RESET INPUT
READY	READY
HRQ	HOLD REQUEST (TO 8080A)
HLDA	HOLD ACKNOWLEDGE (FROM 8080A)

AEN	ADDRESS ENABLE
ADSTB	ADDRESS STROBE
TC	TERMINAL COUNT
MARK	MODULO 128 MARK
DRQ_3-DRQ_0	DMA REQUEST INPUT
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA ACKNOWLEDGE OUT
$\overline{CS}$	CHIP SELECT
V_{CC}	+5 VOLTS
GND	GROUND

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . – 55°C to 125°C
Storage Temperature . . . . . – 65°C to + 150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = – 55°C to 125°C, V_{CC} = + 5V ± 10%, GND = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	Volts	
V_{IH}	Input High Voltage	2.2	V_{CC}+.5	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	Volts	I_{OH}=-150μA for AB, DB and AEN I_{OH}=-80μA for others
V_{HH}	HRQ Output High Voltage	3.3	V_{CC}	Volts	I_{OH} = -80μA
I_{CC}	V_{CC} Current Drain		150	mA	
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Leakage During Float		±10	μA	V_{OUT} = V_{CC} to 0V

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

A.C. CHARACTERISTICS: PERIPHERAL (SLAVE) MODE

$T_A = -55°C$ to $125°C$, $V_{CC} = 5.0V \pm 10\%$; GND = 0V (Note 1).

8080 Bus Parameters

Read Cycle:

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
T_{AR}	Adr or $\overline{CS}\downarrow$ Setup to $\overline{RD}\downarrow$	0		ns	
T_{RA}	Adr or $\overline{CS}\uparrow$ Hold from $\overline{RD}\uparrow$	0		ns	
T_{RD}	Data Access from $\overline{RD}\downarrow$	0	300	ns	(Note 2)
T_{DF}	DB→Float Delay from $\overline{RD}\uparrow$	20	150	ns	
T_{RR}	$\overline{RD}$ Width	250		ns	

Write Cycle:

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
T_{AW}	Adr Setup to $\overline{WR}\downarrow$	20		ns	
T_{WA}	Adr Hold from $\overline{WR}\uparrow$	35		ns	
T_{DW}	Data Setup to $\overline{WR}\uparrow$	200		ns	
T_{WD}	Data Hold from $\overline{WR}\uparrow$	0		ns	
T_{WW}	$\overline{WR}$ Width	175		ns	

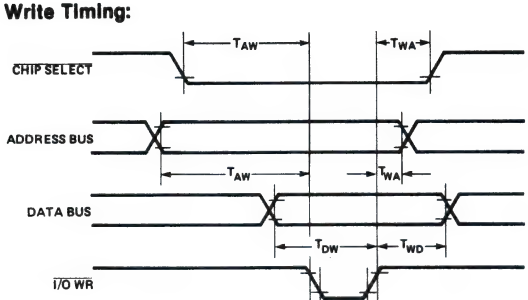
Other Timing:

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
T_{RSTW}	Reset Pulse Width	300		ns	
T_{RSTD}	Power Supply↑ (V_{CC}) Setup to Reset↓	500		μs	
T_r	Signal Rise Time		20	ns	
T_f	Signal Fall Time		20	ns	
T_{RSTS}	Reset to First $\overline{I/O}\overline{WR}$	2		t_{CY}	

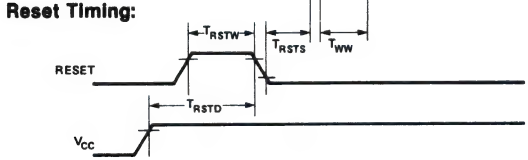
Notes: 1. All timing measurements are made at the following reference voltages unless specified otherwise: Input "1" at 2.0V, "0" at 0.8V
Output "1" at 2.0V, "0" at 0.8V
2. M8257: $C_L = 100$ pF, 8257-5: $C_L = 150$ pF.

M8257 PERIPHERAL MODE TIMING DIAGRAMS

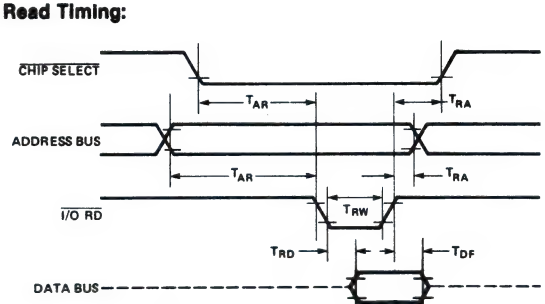
Write Timing:



Reset Timing:



Read Timing:



Input Waveform for A.C. Tests:

A.C. CHARACTERISTICS: DMA (MASTER) MODE

$T_A = -55°C$ to $125°C$, $V_{CC} = +5V \pm 10\%$, GND = 0V

Timing Requirements

Symbol	Parameter	Min.	Max.	Unit
T_{CY}	Cycle Time (Period)	0.320	4	μs
T_θ	Clock Active (High)	120	$.8T_{CY}$	ns
T_{QS}	DRQ↑ Setup to θ↓ (SI, S4)	120		ns
T_{QH}	DRQ↓ Hold from HLDA↑[4]	0		ns
T_{HS}	HLDA↑ or ↓Setup to θ↓ (SI, S4)	100		ns
T_{RS}	READY Setup Time to θ↑ (S3, Sw)	30		ns
T_{RH}	READY Hold Time from θ↑ (S3, Sw)	20		ns

Note: 4. Tracking Parameter.

Tracking Parameters

Signals labeled as Tracking Parameters (footnotes 4-7 under A.C. Specifications) are signals that follow similar paths through the silicon die. The propagation speed of these signals varies in the manufacturing process but the relationship between all these parameters is constant. The variation is less than or equal to 50 ns.

Suppose the following timing equation is being evaluated,

$$T_{A(MIN)} + T_{B(MAX)} \leq 150 \text{ ns}$$

and only minimum specifications exist for T_A and T_B. If $T_{A(MIN)}$ is used, and if T_A and T_B are tracking parameters, $T_{B(MAX)}$ can be taken as $T_{B(MIN)}$ + 50 ns.

$$T_{A(MIN)} + (T_{B(MIN)}^* + 50 \text{ ns}) \leq 150 \text{ ns}$$

*if T_A and T_B are tracking parameters

A.C. CHARACTERISTICS: DMA (MASTER) MODE

$T_A = -55°C$ to $125°C$, $V_{CC} = +5V \pm 10\%$, GND = 0V

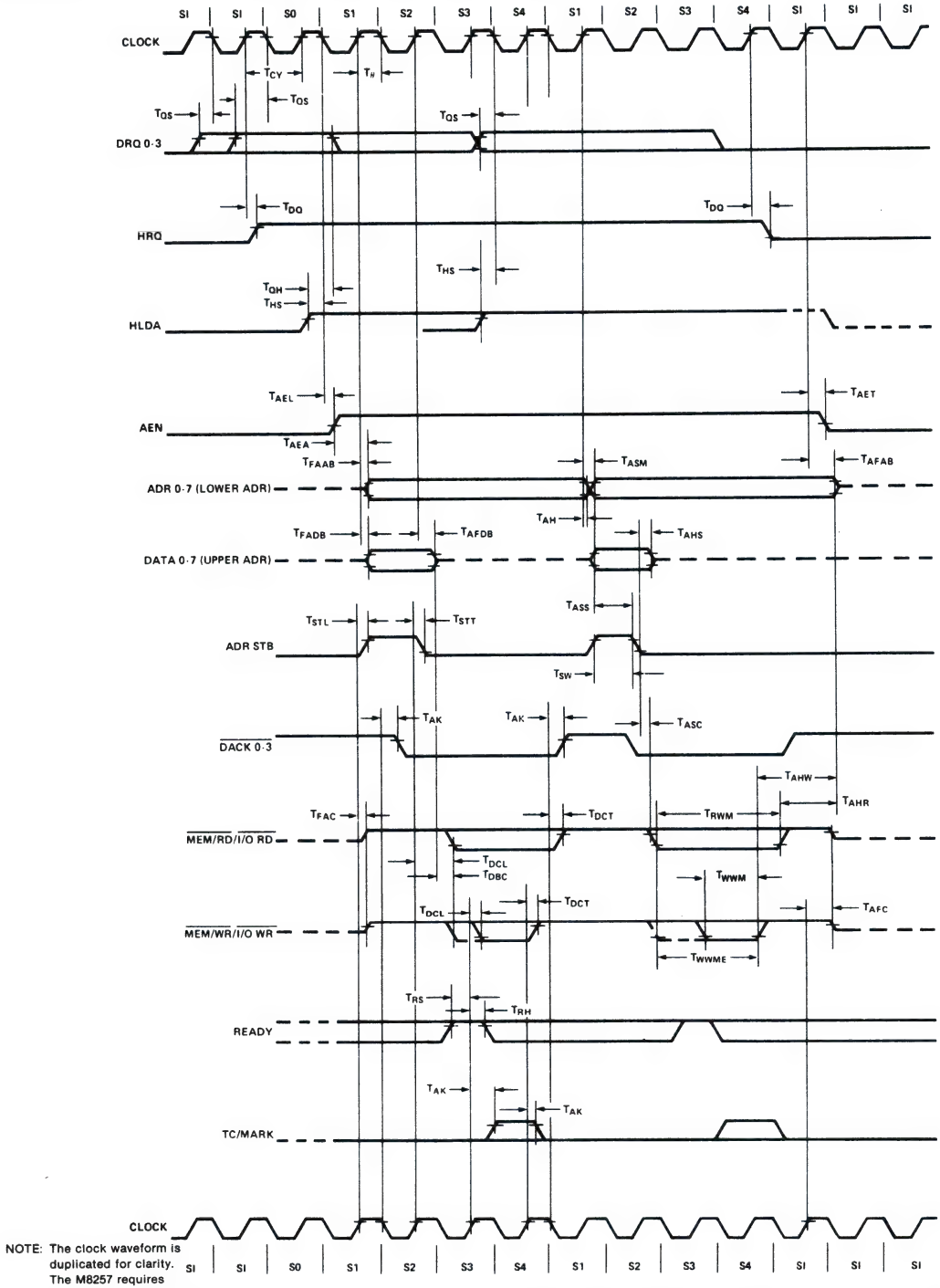
Timing Responses

Symbol	Parameter	Min.	Max.	Unit
T_{DQ}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 2.0V)[1]		180	ns
T_{DQ1}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 3.3V)[3]		270	ns
T_{AEL}	AEN↑ Delay from θ↓(S1)[1]		300	ns
T_{AET}	AEN↓ Delay from θ↑(SI)[1]		200	ns
T_{AEA}	Adr(AB)(Active) Delay from AEN↑(S1)[4]	20		ns
T_{FAAB}	Adr(AB)(Active) Delay from θ↑(S1)[2]		270	ns
T_{AFAB}	Adr(AB)(Float) Delay from θ↑(SI)[2]		200	ns
T_{ASM}	Adr(AB)(Stable) Delay from θ↑(S1)[2]		250	ns
T_{AH}	Adr(AB)(Stable) Hold from θ↑(S1)[2]	$T_{ASM} - 50$		ns
T_{AHR}	Adr(AB)(Valid) Hold from $\overline{Rd}$↑(S1, SI)[4]	60		ns
T_{AHW}	Adr(AB)(Valid) Hold from $\overline{Wr}$↑(S1, SI)[4]	300		ns
T_{FADB}	Adr(DB)(Active) Delay from θ↑(S1)[2]		300	ns
T_{AFDB}	Adr(DB)(Float) Delay from θ↑(S2)[2]	$T_{STT} + 20$	250	ns
T_{ASS}	Adr(DB) Setup to AdrStb↓(S1-S2)[4]	100		ns
T_{AHS}	Adr(DB)(Valid) Hold from AdrStb↓(S2)[4]	50		ns
T_{STL}	AdrStb↑ Delay from θ↑(S1)[1]		200	ns
T_{STT}	AdrStb↓Delay from θ↑(S2)[1]		160	ns
T_{SW}	AdrStb Width (S1-S2)[4]	$T_{CY} - 100$		ns
T_{ASC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from AdrStb↓(S2)[4]	70		ns
T_{DBC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from Adr(DB) (Float)(S2)[4]	20		ns
T_{AK}	DACK↑ or ↓Delay from θ↓(S2, S1) and TC/Mark↑ Delay from θ↑(S3) and TC/Mark↓ Delay from θ↑(S4)[1,5]		270	ns
T_{DCL}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from θ↑(S2) and $\overline{Wr}$↓ Delay from θ↑(S3)[2,6]		250	ns
T_{DCT}	$\overline{Rd}$↑ Delay from θ↓(S1, SI) and $\overline{Wr}$↑ Delay from θ↑(S4)[2,7]		200	ns
T_{FAC}	$\overline{Rd}$ or $\overline{Wr}$(Active) from θ↑(S1)[2]		300	ns
T_{AFC}	$\overline{Rd}$ or $\overline{Wr}$(Float) from θ↑(SI)[2]		170	ns
T_{RWM}	$\overline{Rd}$ Width (S2-S1 or SI)[4]	$2T_{CY} + T_\theta - 50$		ns
T_{WWM}	$\overline{Wr}$ Width (S3-S4)[4]	$T_{CY} - 50$		ns
T_{WWME}	$\overline{Wr}$(Ext) Width (S2-S4)[4]	$2T_{CY} - 50$		ns

Notes: 1. Load = 1 TTL. 2. Load = 1 TTL + 50 pF. 3. Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V. 4. Tracking Parameter.
5. $\Delta T_{AK} < 50$ ns. 6. $\Delta T_{DCL} < 50$ ns. 7. $\Delta T_{DCT} < 50$ ns.

DMA MODE WAVEFORMS

CONSECUTIVE CYCLES AND BURST MODE SEQUENCE



NOTE: The clock waveform is duplicated for clarity. The M8257 requires only one clock input.

Figure 1. Consecutive Cycles and Burst Mode Sequence

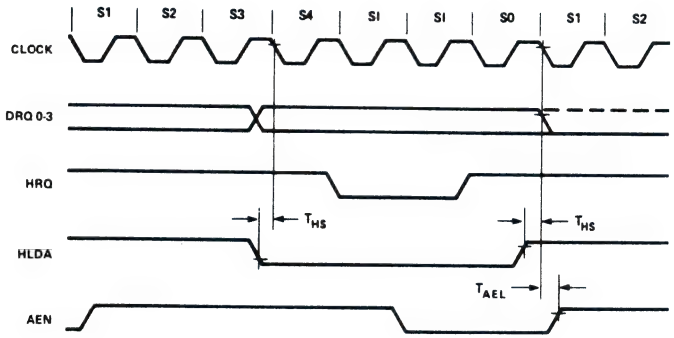


Figure 2. Control Override Sequence

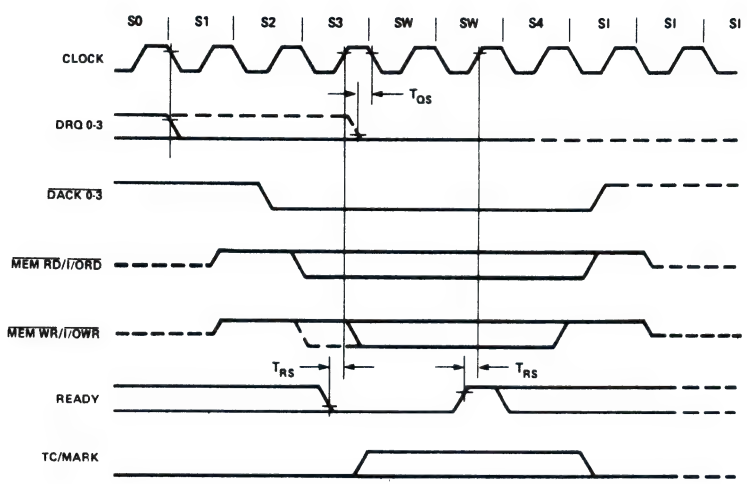


Figure 3. Not Ready Sequence

M8259A
PROGRAMMABLE INTERRUPT CONTROLLER

MILITARY

- **iAPX 86, 88 Compatible**
- **MCS-80®, MCS-85® Compatible**
- **Eight-Level Priority Controller**
- **Expandable to 64 Levels**
- **Programmable Interrupt Modes**
- **Individual Request Mask Capability**
- **Single +5V Supply (No Clocks)**
- **−55°C to +125°C Temp. Range**

The Intel® M8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The M8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

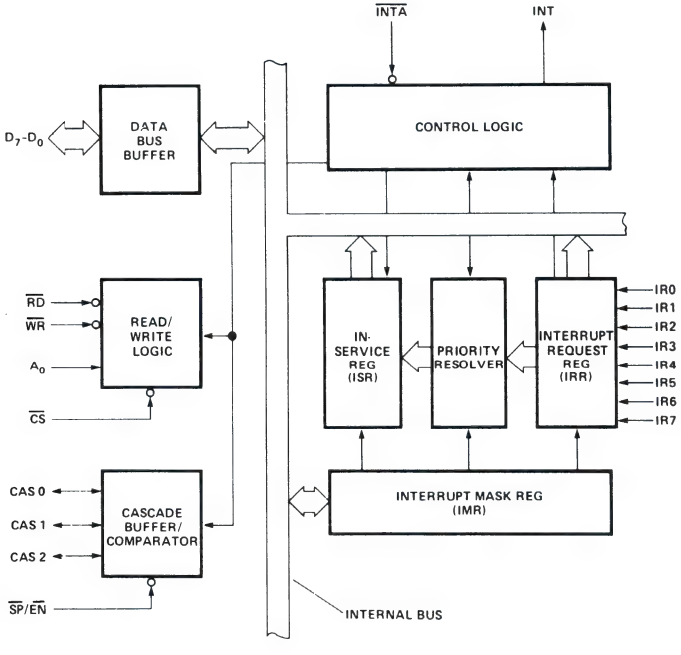


Figure 1. Block Diagram

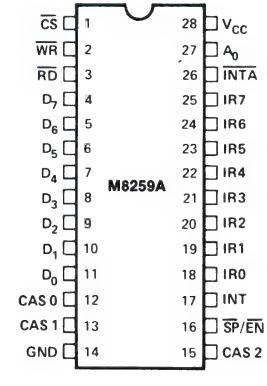


Figure 2. Pin Configuration

Table 1. Pin Names

$D_7 - D_0$	DATA BUS (BI-DIRECTIONAL)
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A_0	COMMAND SELECT ADDRESS
$\overline{CS}$	CHIP SELECT
CAS2-CAS0	CASCADE LINES
$\overline{SP}/\overline{EN}$	SLAVE PROGRAM INPUT/ENABLE
INT	INTERRUPT OUTPUT
$\overline{INTA}$	INTERRUPT ACKNOWLEDGE INPUT
IR0 - IR7	INTERRUPT REQUEST INPUTS

Table 2. Pin Descriptions

Symbol	I/O	Pin #	Function
V_{CC}		28	+5V supply.
GND		14	Ground.
D_{0-7}	I/O	11-4	Bidirectional data bus, used for: a) programming the mode of the 8259A (programming is done by software); b) the microprocessor can read the status of the 8259A; c) the 8259A will send vectoring data to the microprocessor when an interrupt is acknowledged.
IR_{0-7}	I	18-25	Interrupt Requests: These are asynchronous inputs. A positive-going edge will generate an interrupt request. Thus a request can be generated by raising the line and holding it high until acknowledged, or by a negative pulse. In level triggered mode, no edge is required. These lines are active HIGH.
$\overline{RD}$	I	3	Read (generally from 8228 in MCS-80 system or from 8086 in MCS-86 system).
$\overline{WR}$	I	2	Write (generally from 8228 in MCS-80 sytem or from 8086 in MCS-86 system).
$\overline{INTA}$	I	26	Interrupt Acknowledge (generally from 8228 in MCS-80 system, 8086 in MCS-86 system). The 8288 generates three distinct $\overline{INTA}$ pulses when a CALL is inserted, the 8086 produces two distinct $\overline{INTA}$ pulses during an interrupt cycle.
$\overline{CS}$	I	1	Chip Select: $\overline{RD}$ and $\overline{WR}$ are enabled by Chip Select, whereas Interrupt Acknowledge is independent of Chip Select.
A0	I	27	Usually the least significant bit of the microprocessor address output. When A0 = 1 the Interrupt Mask Register can be loaded or read. When A0 = 0 the 8259A mode can be programmed or its status can be read. $\overline{CS}$ is active LOW.
INT	O	17	Goes directly to the microprocessor interrrupt input. This output will have high V_{OH} to match the 8080 3.3V V_{IH}. INT is active HIGH.
C0-C2	I/O	12 13 15	Three cascade lines, outputs in master mode and inputs in slave mode. The master issues the binary code of the acknowledged interrupt level on these lines. Each slave compares this code with its own.
$\overline{SP}/\overline{EN}$	I/O	16	$\overline{SP}/\overline{EN}$ is a dual function pin. In the buffered mode $\overline{SP}/\overline{EN}$ is used to enable bus transceivers ($\overline{EN}$). In the non-buffered mode $\overline{SP}/\overline{EN}$ determines if this 8259A is a master or a slave. If $\overline{SP}$ = 1 the 8259A is master; $\overline{SP}$ = 0 indicates a slave.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... −55°C to 125°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS

T_A = −55°C to 125°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−.5	.8	V	
V_{IH}	Input High Voltage	2.3	V_{CC} + .5V	V	
V_{OL}	Output Low Voltage		.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
$V_{OH(INT)}$	Interrupt Output High Voltage	3.5 2.4		V V	I_{OH} = −100 μA I_{OH} = −400 μA
I_{LI}	Input Load Current		10	μA	V_{IN} = V_{CC} to 0V
I_{LOL}	Output Leakage Current		−10	μA	V_{OUT} = 0.45V
I_{LOH}	Output Leakage Current		10	μA	V_{OUT} = V_{CC}
I_{CC}	V_{CC} Supply Current		85	mA	

8259A A.C. CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$

TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TAHRL	A0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$↓	0		ns	
TRHAX	A0/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$↑	0		ns	
TRLRH	$\overline{RD}$ Pulse Width	235		ns	
TAHWL	A0/$\overline{CS}$ Setup to $\overline{WR}$↓	0		ns	
TWHAX	A0/$\overline{CS}$ Hold after $\overline{WR}$↑	0		ns	
TWLWH	$\overline{WR}$ Pulse Width	290		ns	
TDVWH	Data Setup to $\overline{WR}$↑	240		ns	
TWHDX	Data Hold after $\overline{WR}$↑	0		ns	
TJLJH	Interrupt Request Width (Low)	100		ns	See Note 1
TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$↓ (Slave Only)	55		ns	
TRHRL	End of $\overline{RD}$ to Next Command	300		ns	
TWHRL	End of $\overline{WR}$ to Next Command	370		ns	

Note 1: This is the low time required to clear the input latch in the edge triggered mode.

TIMING RESPONSES

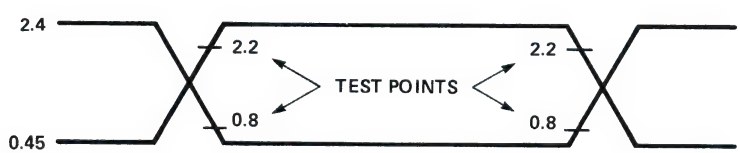
Symbol	Parameter	Min.	Max.	Units	Test Conditions
TRLDV	Data Valid from $\overline{RD}$/$\overline{INTA}$↓		200	ns	C of Data Bus Max. test C = 100 pF Min. test C = 15 pF C_{INT} = 100 pF C_{ENABLE} = 15 pF
TRHDZ	Data Float after $\overline{RD}$/$\overline{INTA}$↑	10	100	ns	
TJHIH	Interrupt Output Delay		350	ns	
TIALCV	Cascade Valid from First $\overline{INTA}$↓ (Master Only)		565	ns	
TRLEL	Enable Active from $\overline{RD}$↓ or $\overline{INTA}$↓		125	ns	
TRHEH	Enable Inactive from $\overline{RD}$↑ or $\overline{INTA}$↑		150	ns	
TAHDV	Data Valid from Stable Address		200	ns	
TCVDV	Cascade Valid to Valid Data		300	ns	

CAPACITANCE

$T_A = 25°C$; $V_{CC} = GND = 0V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

Input Waveforms for A.C. Tests



Notes

Notes

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